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| 4 | 31 | ((detect$3 with (bus near2 (voltage or power)) with suppl$3)) and 713/$3 | USPAT; US-PGPUB |
| 5 | 7 | "6128743" | USPAT; US-PGPUB |
| 6 | 1 | "5675813".PN. | USPAT |
| 7 | 1 | "5799196".PN. | USPAT |
| 8 | 40 | ((detect$3 with (bus near2 (voltage or power)))) and 713/$3 and ieee | USPAT; US-PGPUB |
| 9 | 76 | (select$3 adj2 (power adj (source or supply))) same (detect$3 near2 (voltage or power)) | USPAT; US-PGPUB |
| 10 | 3 | (select$3 adj2 (power adj (source or supply))) same (detect$3 near2 (voltage or power)) same bus | USPAT; US-PGPUB |
| 11 | 824 | ((us$3 or utiliz$5) near3 (bus near2 power)) | USPAT; US-PGPUB |
| 12 | 36 | ((us$3 or utiliz$5) near3 (bus near2 power)) with (detect$3 or determin$5) | USPAT; US-PGPUB |
| 13 | 25 | (switch$3 with (bus near2 power)) with suppl$3 with detect$3 | USPAT; US-PGPUB |
| 14 | 1 | regan.in. and miller.in. | USPAT; US-PGPUB |
| 15 | 10 | (switch$3 with (bus near2 power)) with suppl$3 with detect$3 | EPO; JPO |
| 16 | 46 | (select$3 adj2 (power adj (source or supply))) same (detect$3 near2 (voltage or power)) | EPO; JPO |
| 17 | 2 | ((select$3 adj2 (power adj (source or supply))) same (detect$3 near2 (voltage or power))) and bus | EPO; JPO |

US006357011B2

(12) **United States Patent**
**Gilbert**

(10) **Patent No.: US 6,357,011 B2**
(45) **Date of Patent: *Mar. 12, 2002**

(54) **BUS-POWERED COMPUTER PERIPHERAL WITH SUPPLEMENT BATTERY POWER TO OVERCOME BUS-POWER LIMIT**

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(73) Assignee: **Gateway, Inc.**, N. Sioux, SD (US)

( * ) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/115,843**

(22) Filed: **Jul. 15, 1998**

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(52) **U.S. Cl.** ..... **713/300**; 713/310; 713/320; 320/34

(58) **Field of Search** ..... 713/300, 310, 713/320; 709/238; 702/122; 326/34; 400/88

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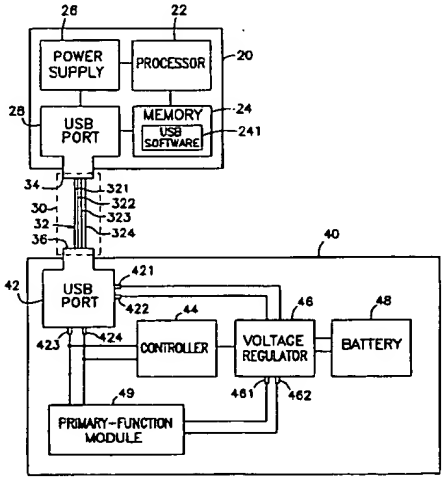
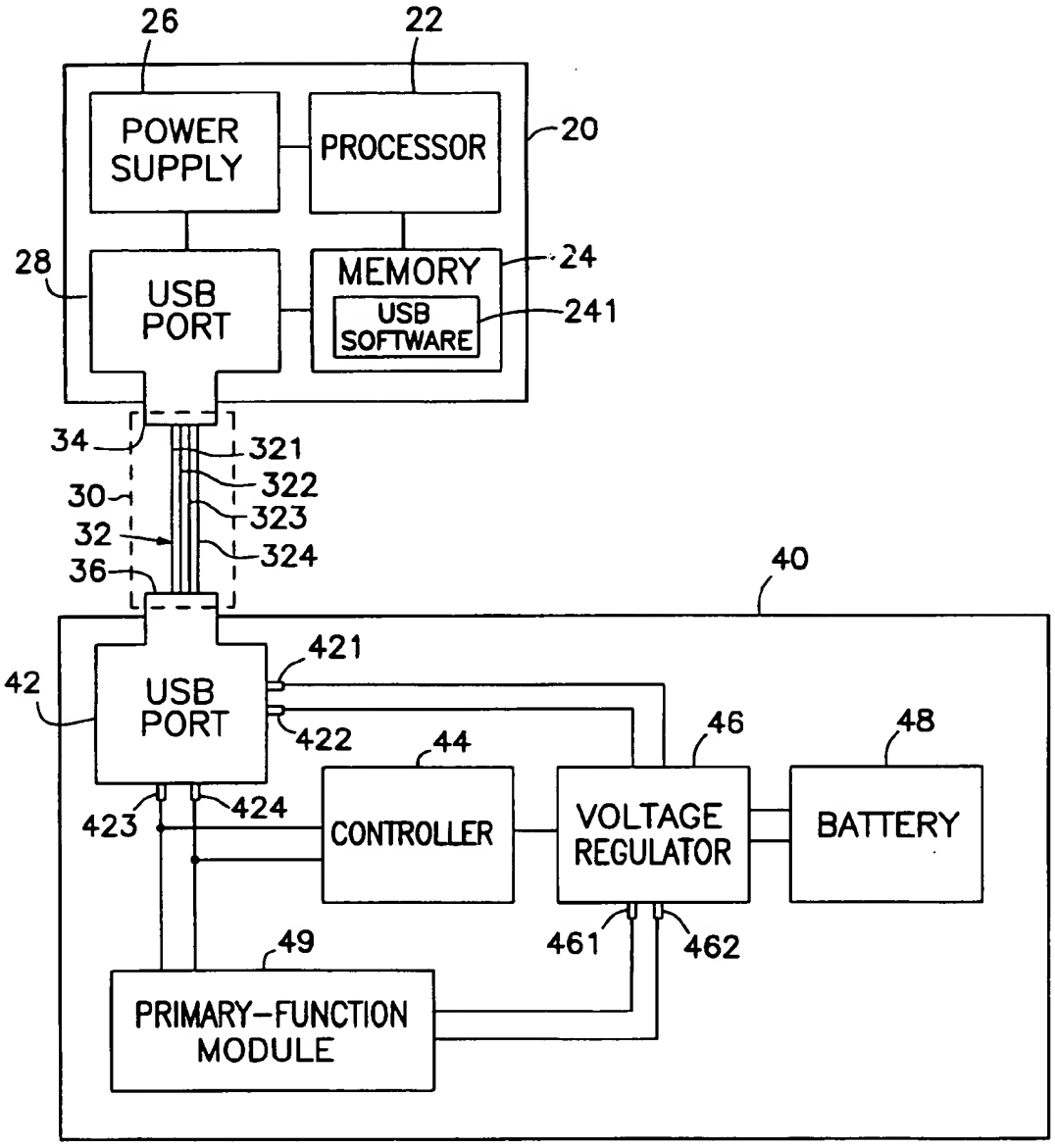
*Primary Examiner*—Ayaz Sheikh
*Assistant Examiner*—Frantz B. Jean
(74) *Attorney, Agent, or Firm*—Kenneth Cool; Eduardo E. Drake; Schwegman Lundberg Woesnner & Kluth

(57) **ABSTRACT**

A computer system typically includes a central computer and several peripherals, such as a mouse and a printer, which communicate with the computer via a communications channel known as a serial bus. The serial bus may also supply a limited amount of power to some peripherals. Unfortunately, the power limit compels high-power peripherals to include independent power supplies, an arrangement which increase their complexity and cost. Accordingly, one embodiment of the present invention provides a bus-powered peripheral that includes a controller, a rechargeable battery, and a voltage regulator or recharge circuit. The recharge circuit monitors data on a serial bus, recharges the battery during inactive periods, and allows the battery to supplement bus power during active periods, thereby overcoming the power limit of the serial bus.

**12 Claims, 3 Drawing Sheets**

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20
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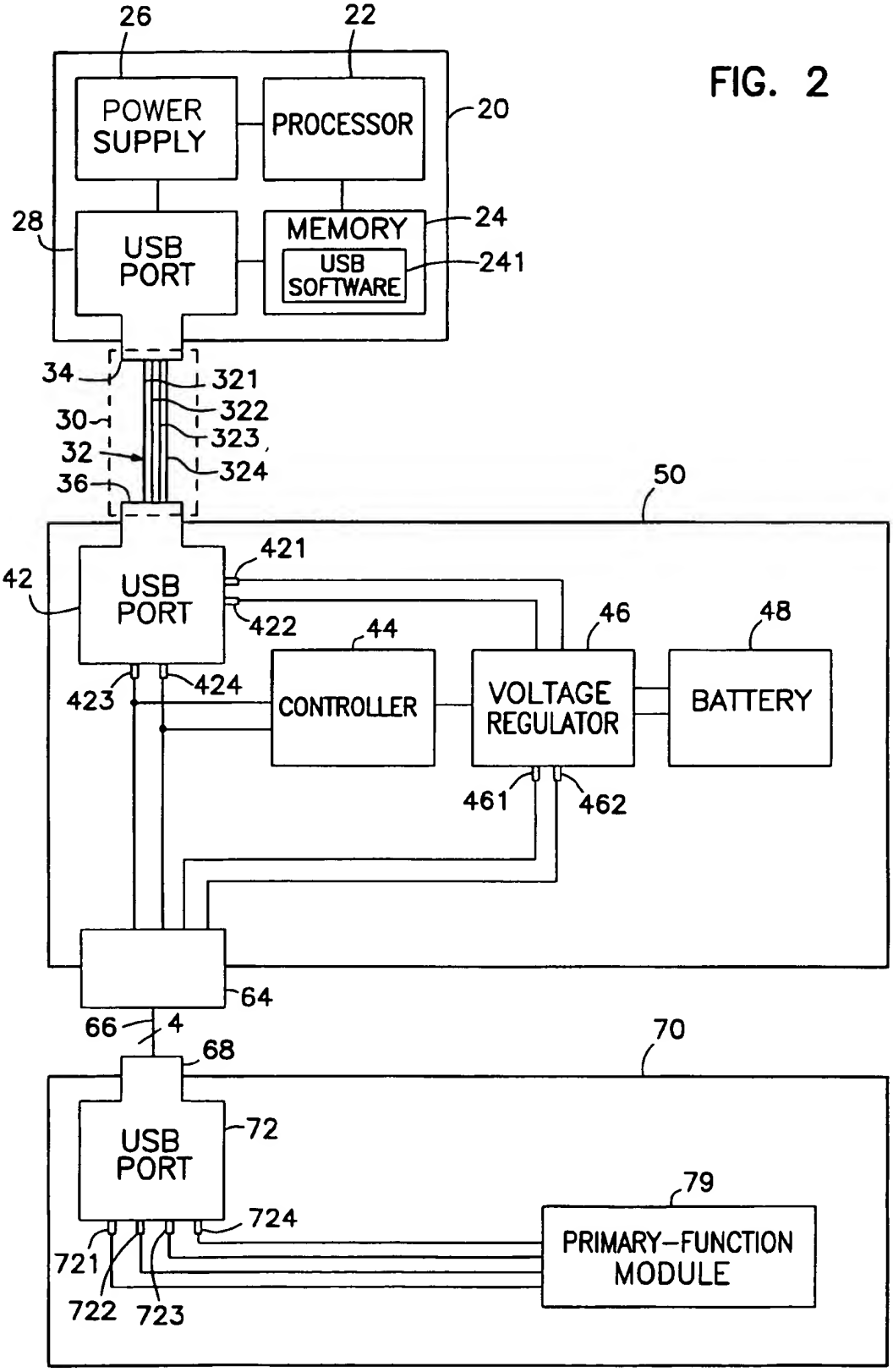
USB PORT
MEMORY
24
USB SOFTWARE
241
34
321
322
323
324
30
32
36
40
421
42
USB PORT
422
44
46
48
423
424
CONTROLLER
VOLTAGE REGULATOR
BATTERY
49
461
462
PRIMARY-FUNCTION MODULE

FIG. 1

FIG. 2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MEMORY
24
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241
34
321
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322
323
32
324
36
50
42
USB PORT
421
422
44
46
48
423
424
CONTROLLER
VOLTAGE REGULATOR
BATTERY
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462
64
66
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68
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USB PORT
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724
PRIMARY-FUNCTION MODULE
721
722
723

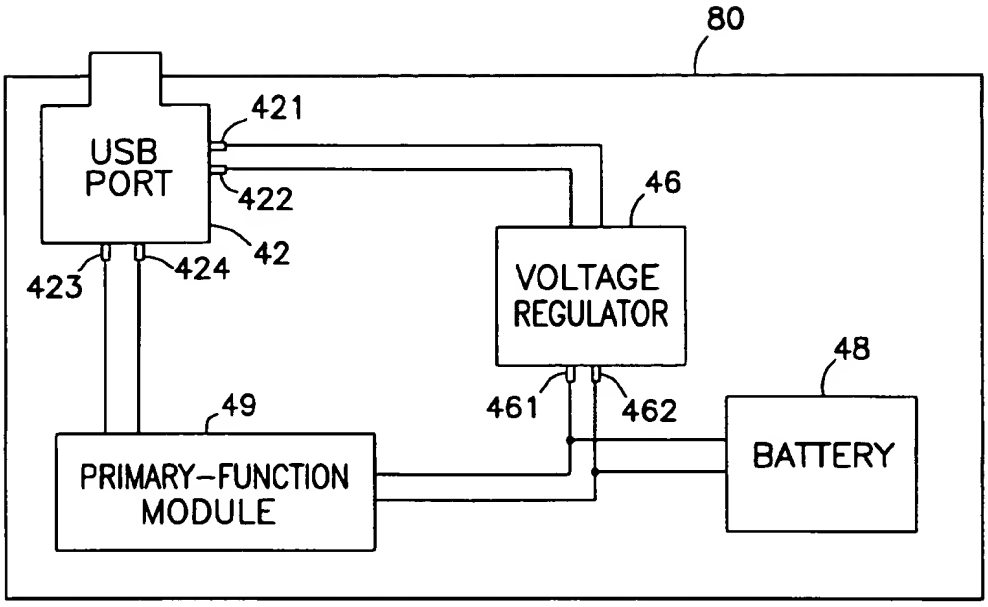
80
421
USB PORT
422
42
423
424
46
VOLTAGE REGULATOR
48
49
461
462
PRIMARY-FUNCTION MODULE
BATTERY

FIG. 3

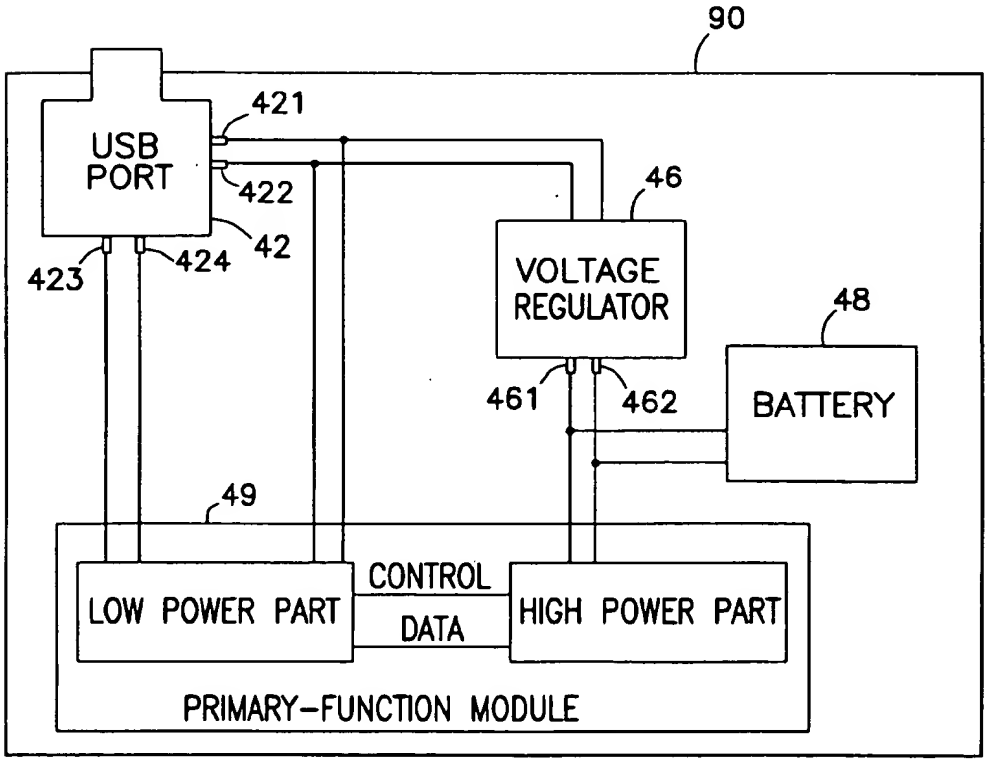
90
421
USB PORT
422
42
423
424
46
VOLTAGE REGULATOR
48
461
462
BATTERY
49
CONTROL
LOW POWER PART
DATA
HIGH POWER PART
PRIMARY-FUNCTION MODULE

FIG. 4

# BUS-POWERED COMPUTER PERIPHERAL WITH SUPPLEMENT BATTERY POWER TO OVERCOME BUS-POWER LIMIT

## FIELD OF THE INVENTION

The present invention concerns computer systems and computer peripherals, particularly a system that recharges a battery-powered peripheral through a serial bus.

## BACKGROUND OF THE INVENTION

Computer systems, particularly personal computers, typically include a central processing unit and a number of peripherals, or auxiliary devices, such as monitors, keyboards, mice, disc drives, printers, scanners, and even cameras, which communicate with the central processing unit. The central processing unit and the peripheral devices are usually connected via a two-way communications channel, known as a serial bus, which carries a stream of electrical pulses representing a sequence of ones and zeros. The serial bus may also carry electrical power for operating one or more peripherals.

Serial bus parameters, or specifications, are usually standardized not only to reduce the number of communications protocols, or procedures, a computer must understand, but also to simplify matching of computers and peripherals. Examples of serial bus specifications include Apple desktop bus (ADB), Access.bus (A.b), Institute of Electrical and Electronic Engineers (IEEE) P1394, Concentration Highway Interface (CHI), and GeoPort.

Within the past few years, a new serial bus specification, called the Universal Serial Bus (USB) Specification, has been developed to work with peripherals that require higher data rates, more flexibility, or less complexity than previously available in standard serial busses. A Universal Serial Bus, a serial bus that operates according to the USB Specification, has a maximum data rate of 12 million bits per second (12 Mbps), and carries as much as 2.5 watts of electric power to operate USB peripherals (that is, USB-compliant peripherals).

One problem with the USB and other serial bus specifications are the power limits they impose on bus-powered peripherals, peripherals that operate almost entirely on power carried by a serial bus. Because of the power limits, high-power peripherals, such as printers or speakers, that require more than the power limit for a particular serial bus must use separate, external power supplies. Unfortunately, external power supplies add expense and complexity to peripherals.

Accordingly, there is a need for a better way of powering high-power computer peripherals.

## SUMMARY OF THE INVENTION

To address this and other needs, the present invention provides a peripheral with a rechargeable battery that stores energy during inactive periods for use during active periods. In one exemplary embodiment, the peripheral includes a voltage regulator for coupling to a pair of bus power lines; a controller coupled between the voltage regulator and one or more bus data lines; and a rechargeable battery coupled to the voltage regulator. In operation, the controller switches the battery between a charge mode and a supply mode according to signals received through the bus data lines. The charged battery supplements the power available through the bus power lines, thereby providing more power for operating the peripheral than otherwise available over the bus power lines alone.



Another embodiment packages the supplemental power capabilities as a power-extension or power-enhancement peripheral for connection between a computer and another peripheral. And, yet another embodiment, which lacks a controller, relies on rechargeable battery coupled in parallel with a primary-function module of the peripheral. The rechargeable battery responds automatically to power demands of the primary-function module to supply supplemental power during high-power-demand periods and to store excess power during low-power-demand periods.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a first computer system including a computer peripheral with rechargeable battery;

FIG. **2** is a block diagram of a second computer system including a power-extension peripheral connected between a computer and a USB bus-powered peripheral;

FIG. **3** is a block diagram of another embodiment of a computer peripheral having a rechargeable battery; and

FIG. **4** is a block diagram of another embodiment of a computer peripheral having a rechargeable battery.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

The following detailed description, which references and incorporates FIGS. **1–4**, describes and illustrates specific preferred embodiments, or versions, of the invention. These embodiments, offered not to limit but only to exemplify and teach the invention, are shown and described in sufficient detail to enable those skilled in the art to practice the invention. Thus, where appropriate to avoid obscuring the invention, the description may omit certain information known to those of skill in the art.

FIG. 1 shows a personal computer system **10**, which includes a personal computer **20**, a Universal Serial Bus (USB) **30**, and a USB peripheral **40**. Computer **20**, preferably a Gateway 2000 personal computer from Gateway 2000, Inc. of North Sioux City, S. Dak., includes a processor **22**; a memory **24**, which includes Universal Serial Bus (USB) communications software **241**; a power supply **26**, which converts 110 VAC to 5 volts DC; and a USB port **28**, which follows the USB Specification 1.0 (Final Revision of Nov. 13, 1995) or an earlier or subsequent version. The USB Specification is incorporated herein by reference.

USB port **28** connects to USB serial bus **30**. USB serial bus **30** includes a USB cable **32** which terminates at one end (computer end) with USB connector **34** and at its other end (peripheral end) with USB connector **36**. In accord with the USB Specification, cable **32**, which has 90-ohm impedance, includes four insulated wires **321–324**. Wires **321** and **322** provide respective nominal voltages of 5 volts and return ground, and carry a maximum of 2.5 watts of power. Wires **323** and **324** are differential data lines that carry differential data signals as well as an NRZI-encoded clock signal. Connector **34**, at the computer end of cable **32**, mates with USB port **26**, and connector **36**, at the peripheral end, mates with USB port **42** of USB peripheral **40**.

Port **42** includes not only power terminals **421** and **422** which connect respectively to wires **321** and **322**, but also data terminals **423** and **424** which connect respectively to wires **323** and **324**. USB peripheral **40** additionally includes an interface-controller module **44**, a voltage regulator (or recharge circuit) **46**, a rechargeable battery **48**, and a primary-function module **49**. Interface-controller module **44** is connected to data terminals **423** and **424** of USB port **42**.

Power terminals 421 and 422 (of port 42) connect to voltage regulator 46. Voltage regulator 46 connects to battery (or energy-storage device) 48, which includes one or more energy-storage cells (not shown), preferably long-life rechargeable lithium, nickel-cadmium, zinc-bromine, or alkaline-manganese cells with minimum charging hysteresis. In addition, voltage regulator 46 includes output terminals 461 and 462 which are connected to primary-function module 49.

Primary-function module 49 includes the primary circuits and components necessary for the USB peripheral to perform its intended function. For example, USB peripheral 40 may be a printer, and module 49 would thus include the buffers, print heads, motors, etc. for a complete printer. Alternatively, USB peripheral 40 may also be a pair of speakers, with each speaker including a digital-to-analog converter, an amplifier, volume controls, and an audio transducer. Ultimately, the invention encompasses any type of computer peripheral, including high-power peripherals that require more power than available through bus 30.

In operation, interface-controller module 44 monitors and decodes data received at data terminals 423 and 424. If it receives data indicating or invoking an inactive period, for example, data instructing that the peripheral be turned off, it sends a control signal to voltage regulator 46. The control signal invokes a charge mode in voltage regulator 46. In the charge mode, voltage regulator 46 diverts power away from primary-function module 49 to battery 48, thereby charging battery 48.

On the other hand, if interface-controller module 44 receives data indicating or invoking an active period, such as data instructing that the peripheral be turned on, it sends a different control signal to voltage regulator 44. The different control signal invokes a supply mode during which module 44 couples battery 48 to primary function module 49, allowing battery 48 to provide supplemental power to primary-function module 48. Thus, during the supply mode, primary-function module 48 receives power not only from computer 20 (via bus 30), but also from battery 48, thereby overcoming the 2.5-watt power limit of bus 30.

In another embodiment, voltage regulator 46 monitors power drawn by primary-function module 49 against that available through serial bus 30. If excess power is available, that is, if more power is available than power being drawn, voltage regulator 46 invokes a variable-trickle-charge mode which charges battery 49 at a rate proportionate to, or at least dependent on, the amount of excess power. Consequently, battery 49 keeps a charge sufficient to consistently satisfy the peak power demands of primary-function module 48.

FIGS. 2–4 show three other embodiments of the invention. In particular, FIG. 2 shows a system 100 in which USB peripheral 50 functions solely as an in-line power-extension (or power-enhancement) peripheral for a separate high-power peripheral 70. The major difference between peripherals 40 and 50 is that peripheral 50 lacks primary-function module 49 and outputs power and data through a USB connector 64. Connector 64 is connected via a USB cable 66 to another USB connector 68. Connector 68 engages USB port 72 of peripheral 70. Port 72, substantially identical in structure and function to port 42, has four output terminals 721–724 connected to a primary-function module 79. Module 79 is substantially identical in structure and function to module 49.

In operation, the peripheral 50 operates much like peripheral 40. More precisely, port 42 and controller 44 of power-extension peripheral 50 decode and monitor data on bus 30. If controller 44 detects data indicating or invoking an inactive period for peripheral 70, it directs regulator 46 to divert power away from connector 64 and thus away from peripheral 70 to charge battery 48. On the other hand, if controller 44 detects data indicating or invoking an active period for peripheral 70, it allows battery 48 to provide supplemental power through connector 64, cable 66, and connector 68 to peripheral 70, thereby overcoming the 2.5-watt power limit of bus 30. Furthermore, two or more substantially similar power-extension peripherals can be connected in parallel to provide even more supplemental power to a given high-power peripheral.

FIG. 3 shows another embodiment of high-power peripheral 40, designated 80. Peripheral 80 includes many of the same or similar components as peripheral 40, namely USB port 42, voltage regulator 46, battery 48, and primary-function module 49. Notably, peripheral 80 lacks controller 44 for monitoring and detecting bus data indicative of active or inactive operating periods. Instead, peripheral 80 has battery 48 connected in parallel with output terminals 461–462 of voltage regulator 46 to "sense" the current drawn by primary-function module 49. During low power-demand periods, excess bus power (that is, bus current not drawn by module 49) charges battery 48 as necessary, and during high power-demand periods, battery 48 supplies supplemental power to primary-function module 49. Thus, like peripherals 40 and 70, peripheral 80 overcomes the 2.5-watt power limit of bus 30.

FIG. 4 shows another embodiment of high-power peripheral 40, designated 90. Peripheral 90 includes many of the same or similar components as peripheral 40, specifically USB port 42, voltage regulator 46, battery 48, and primary-function module 49. However, primary-function module 49 has been divided, preferably according to power requirements, into two portions: a low-power portion 49*a* which receives power and data only from USB port 42, and a high-power portion 49*b* which receives power from both USB port 42 and battery 48.

Low-power portion 49*a* preferably includes control logic and circuits for operating high-power portion 49*b*, and, high-power portion 49*b* includes one or more transducers for converting electrical energy into another form of energy essential to the function of the peripheral. For example, high-power portion 49*b* could include a motor which converts electrical energy to kinetic energy, or a light source which converts electrical energy to light, or a speaker which converts electrical energy to an acoustic energy. However, the scope of the invention encompasses any convenient division of a peripheral into first and second portions with the second portion connected to receive supplemental battery power.

Peripheral 90 has battery 48 connected in parallel with output terminals 461–462 of voltage regulator 46 to sense the current load of only the high-power portion 49*b*, which is activated or deactivated via a control line from low-power portion 49*a*. Thus, when low-power portion 49*a* activates high-power portion 49*b*, battery 48 supplies supplemental power to primary-function module 49, and when low-power portion 49*b* deactivates high-power portion 49*b*, excess bus power charges battery 48. Therefore, like peripherals 40, 50, and 80, peripheral 90 overcomes the power limit of bus 30.

## CONCLUSION

The present invention provides several embodiments of bus-powered peripherals, including a power-extension peripheral, which overcome the 2.5-watt power limitation

imposed by the USB Specification. Ultimately, the invention, applicable to any communications bus, eliminates the need to provide a separate external power supply in many high-power computer peripherals.

The embodiments described above are intended only to illustrate and teach one or more ways of practicing or implementing the present invention, not to restrict its breadth or scope. The actual scope of the invention, which encompasses all ways of practicing or implementing the invention, is defined only by the following claims and their equivalents.

What is claimed is:

1. A system comprising:

a computer;

a bus having at least a pair of data lines for communicating data and at least a pair of power lines for supplying power according to a predetermined power limit; and

a peripheral coupled to the computer via the bus to receive data and power, the peripheral including:

a rechargeable battery;

a communications port having two power terminals for coupling to the pair of power lines and having two data terminals for coupling to the pair of data lines;

a voltage regulator coupled to the power terminals and the rechargeable battery;

a primary-function module coupled to the voltage regulator; and

a controller coupled to at least one of the two data terminals and to the voltage regulator, the controller responsive to signals at the data terminals, indicating an inactive period, to switch the voltage regulator to a charge mode during which it charges the rechargeable battery and responsive to signals at the data terminals, indicating an active period, to switch the voltage regulator to a battery supply mode during which it transfers energy from the rechargeable battery and from the power lines to the primary-function module, thereby providing the primary-function module power in excess of the predetermined power limit.

2. The computer peripheral of claim 1, wherein the primary-function module includes components of a printer, scanner, fax machine, or speaker.

3. A system comprising:

a computer for processing data;

a bus, coupled to the computer, for communicating data;

a power supply for supplying a limited amount of power;

power-extension means, coupled to the computer via the bus and to the power supply and including a supplemental power source, for supplying more than the limited amount of power; and

a computer peripheral coupled to the bus via the power-extension means to receive power concurrently from the power supply and the supplemental power source, and thus able to receive more than the limited amount of power.

4. The system of claim 3, wherein the power supply is part of the computer.

5. The system of claim 3, wherein the supplemental power source comprises a rechargeable battery and the power-extension peripheral further comprises:

a power terminal coupled to the power supply;

a data terminal coupled to the computer to receive signals;

a voltage regulator coupled to the power terminal and the rechargeable battery, and having an output terminal coupled to the computer peripheral; and

a controller coupled to the voltage regulator and responsive to signals at the data terminal to switch the voltage regulator between a charge mode that connects the rechargeable battery to the power terminal for recharge and a supply mode that connects the rechargeable battery and the power terminal to the output terminal for supplying power concurrently from both the battery and power supply to the computer peripheral.

6. A method of operating a computer peripheral connected to a computer via a bus having a predetermined nominal power limit, the method comprising:

transferring power and data via the bus to the computer peripheral;

operating at least a part of the peripheral with power transferred via the bus; and

charging a battery with at least a portion of the power transferred via the bus; and

concurrently supplying first and second amounts of power to the part of the peripheral, with the first amount transferred via the bus and the second amount derived from the charged battery, and with a sum of the first and second amounts exceeding the nominal power limit.

7. The method of claim 6, wherein operating at least a part of the peripheral and charging the charging the battery occur concurrently.

8. An apparatus comprising:

a peripheral device for communicating with a host device via a peripheral device bus, the peripheral device being capable of communicating with the host device via the peripheral device bus and further being capable of receiving operational power via the peripheral device bus; and

a controller for causing a battery to be charged via the peripheral device bus during a lower power consuming period of the peripheral device, the controller causing the battery to provide supplemental power to the peripheral device in the event the peripheral device requires operational power at a level greater than a specified power limit of the peripheral device bus.

9. An apparatus as claimed in claim 8, wherein while being charged via the peripheral bus, the battery is charged at a rate within the specified power limit of the peripheral device bus.

10. An apparatus as claimed in claim 8, wherein while the peripheral device requires operational power greater than the limit of the peripheral device bus, the battery and the peripheral device bus simultaneously provide operational power to the peripheral device without causing the peripheral device bus to provide power at a level greater than the limit of the peripheral device bus.

11. An apparatus as claimed in claim 8, the peripheral device being capable of operating at a power level greater than the limit of the peripheral device bus without causing the peripheral device bus to provide power beyond the limit by receiving supplemental power from the battery.

12. An apparatus as claimed in claim 8, the controller causing the battery to cease providing supplemental power to the peripheral device in the event the peripheral device requires operational power at a level within the limit of the peripheral device.

* * * * *

US006125455A

# United States Patent [19]

Yeo

[11] Patent Number: 6,125,455

[45] Date of Patent: Sep. 26, 2000

[54] **POWER CONTROL DEVICE AND METHOD FOR USB**

[75] Inventor: **Joung-Hyun Yeo**, Kyungki-do, Rep. of Korea

[73] Assignee: **SamSung Electronics Co., Ltd.**, Kyungki-do, Rep. of Korea

[21] Appl. No.: **09/038,961**

[22] Filed: **Mar. 12, 1998**

[30] **Foreign Application Priority Data**

Mar. 12, 1997 [KR] Rep. of Korea ..... 97-08312

[51] **Int. Cl.**[7] ..... **G06F 11/00**

[52] **U.S. Cl.** ..... **714/14**; 710/126; 713/300

[58] **Field of Search** ..... 395/750; 714/14; 364/707; 710/126, 1, 129; 713/300, 320, 330

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*Primary Examiner*—Robert W. Beausoliel, Jr.
*Assistant Examiner*—Pierre E. Elisca
*Attorney, Agent, or Firm*—Robert E. Bushnell, Esq.

[57] **ABSTRACT**

A universal serial bus (USB) power control device includes a universal serial bus control circuit for controlling mutual information transmitted between a computer and its peripheral devices, using data and clocking signals transmitted from a display, a DC—DC converter for processing a power supplied from the display in order to provide an operational power to the universal serial bus control circuit and the peripheral devices, and a universal serial bus power control circuit for detecting a power supplied to the DC—DC converter from the display. If the power supplied from the monitor to the universal serial bus control circuit is abnormal, the abnormal power supplied from the monitor is replaced by normal power supplied from the computer and a message is displayed on the monitor so that a user can recognize that a power supply supplying power to the universal serial bus has failed.

**20 Claims, 5 Drawing Sheets**

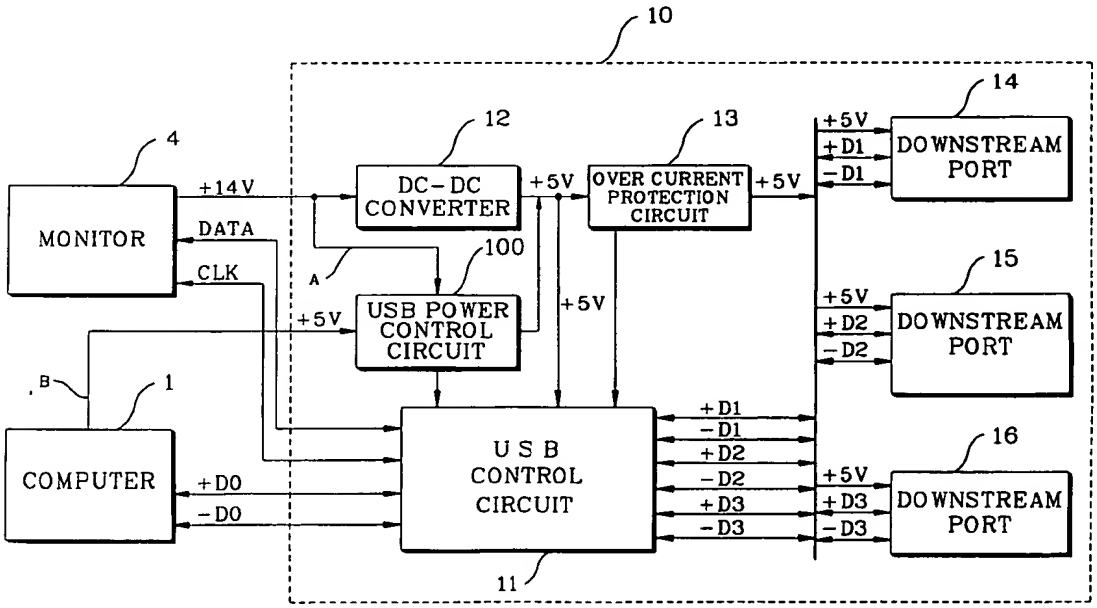


FIG. 1

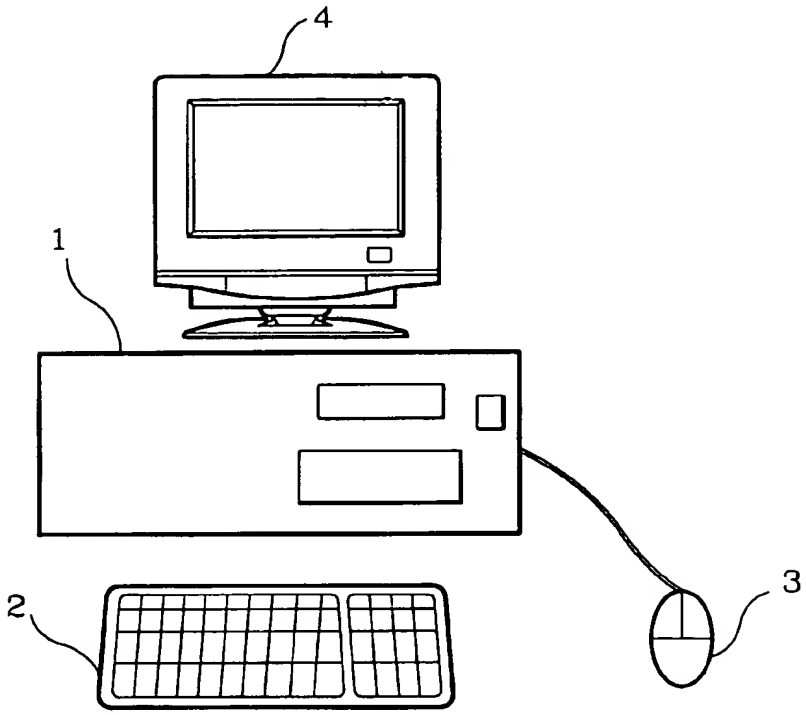



FIG. 2

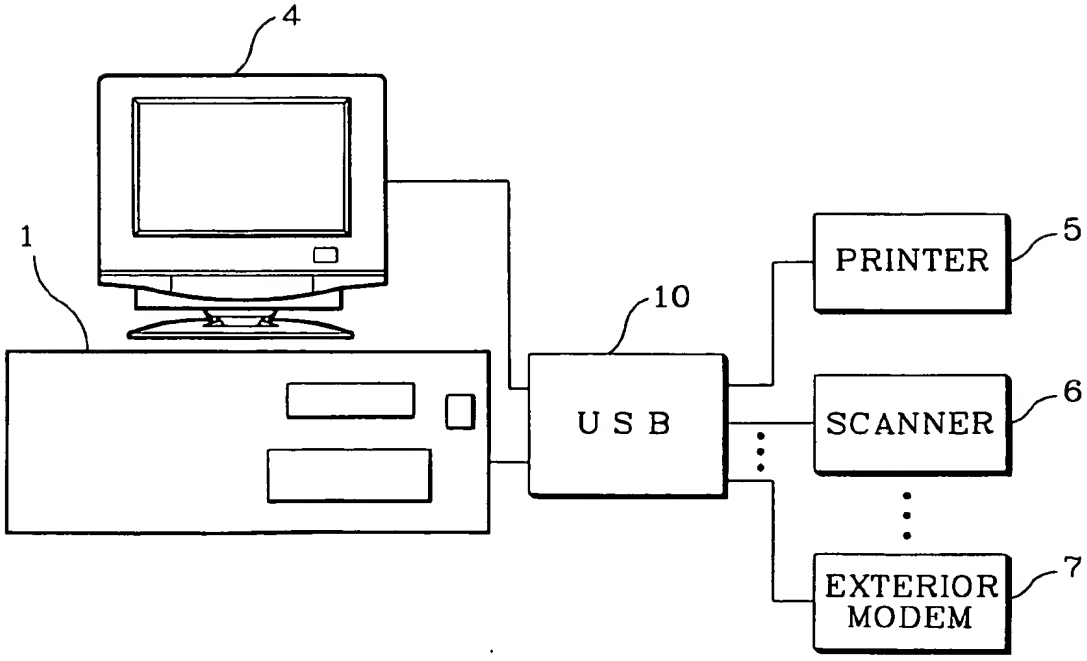


FIG. 3

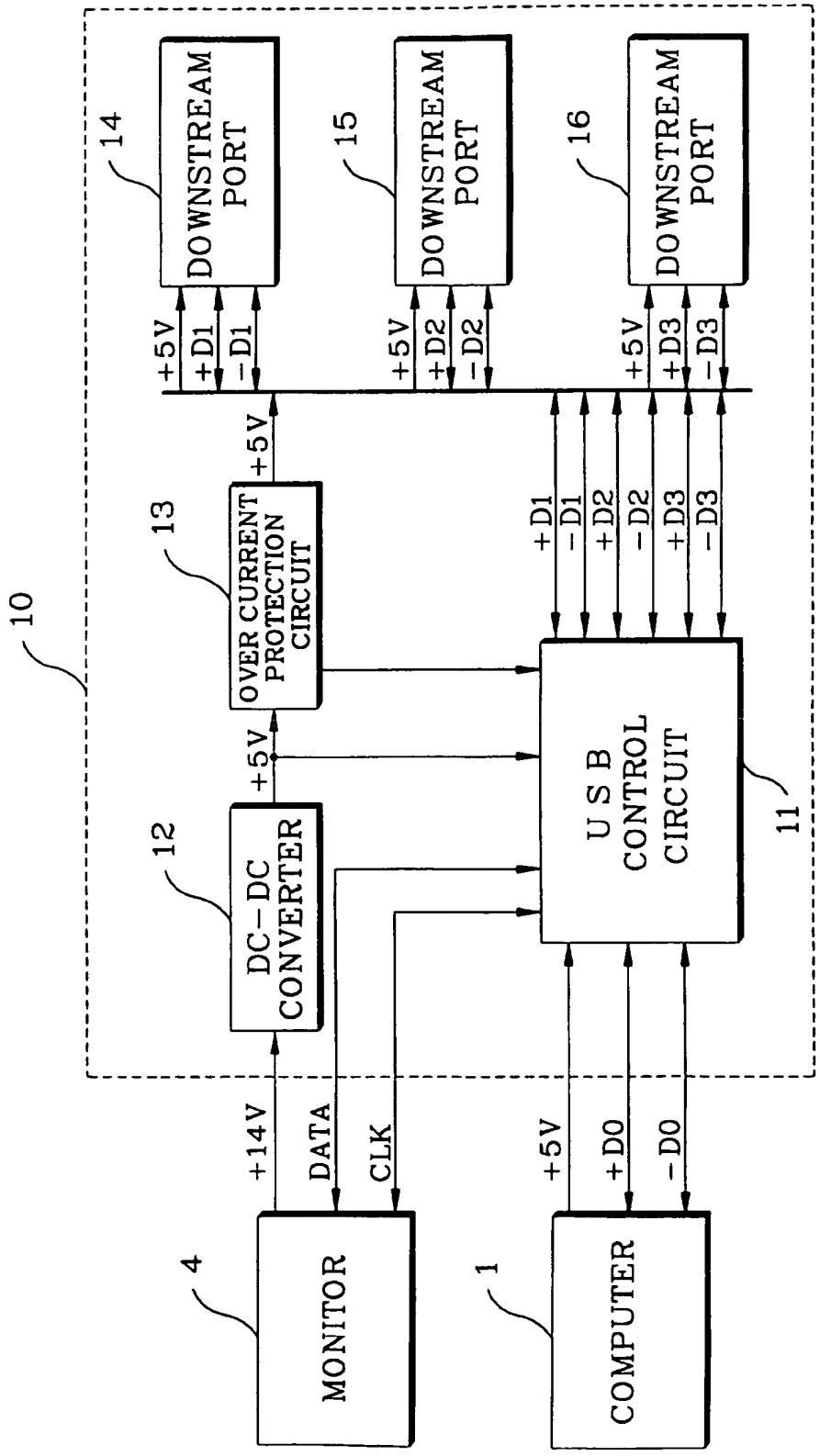

10
11
12
13
14
15
16
4
1
DOWNSTREAM PORT
DOWNSTREAM PORT
DOWNSTREAM PORT
OVER CURRENT PROTECTION CIRCUIT
DC-DC CONVERTER
USB CONTROL CIRCUIT
MONITOR
COMPUTER
+5V
+D1
-D1
+D2
-D2
+D3
-D3
+14V
DATA
CLK
+D0
-D0

FIG. 4

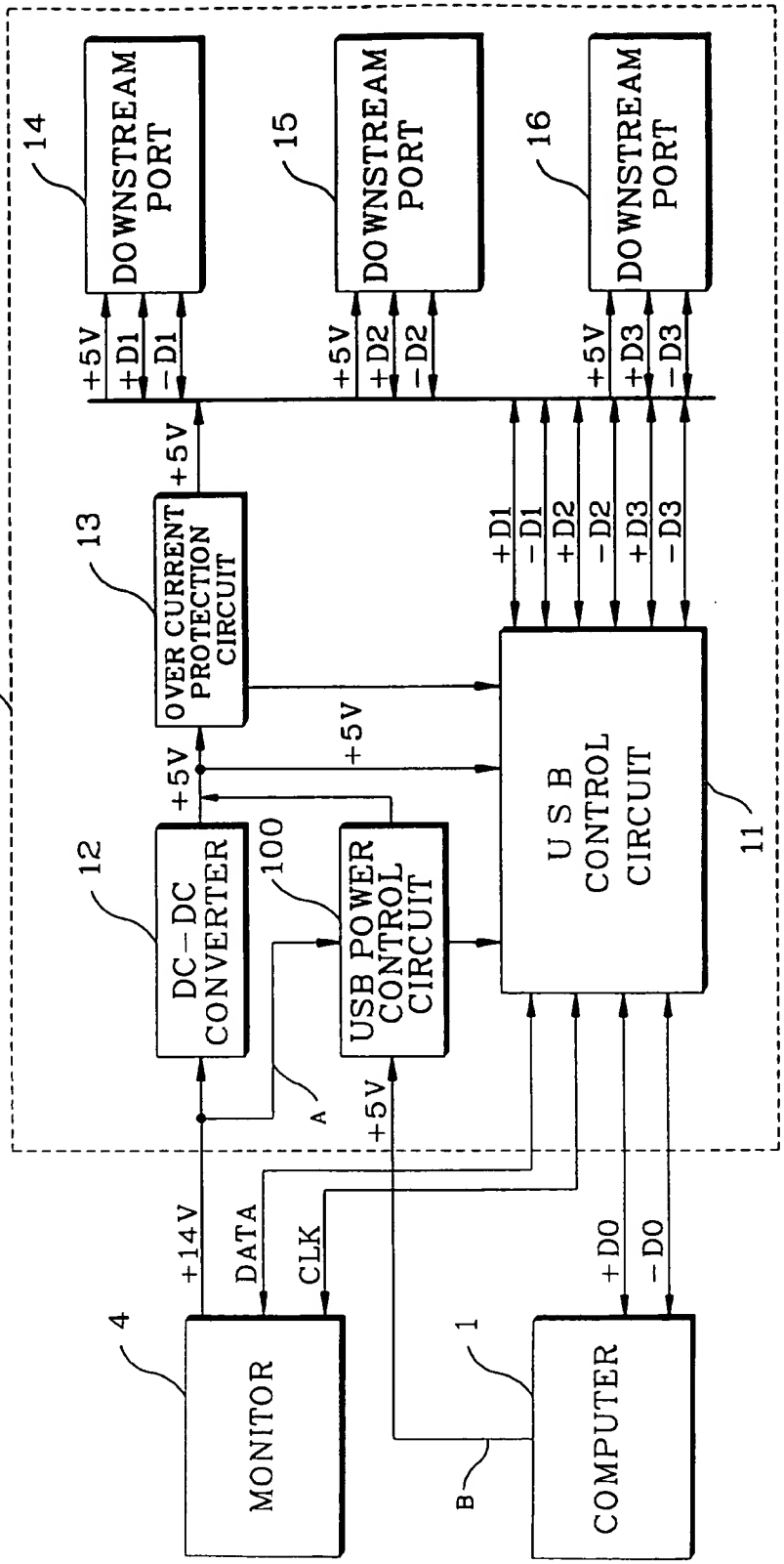

10
14
DOWNSTREAM PORT
15
DOWNSTREAM PORT
16
DOWNSTREAM PORT
+5V
+D1
-D1
+5V
+D2
-D2
+5V
+D3
-D3
13
OVER CURRENT PROTECTION CIRCUIT
+5V
+D1
-D1
+D2
-D2
+D3
-D3
+5V
+5V
12
DC-DC CONVERTER
100
USB POWER CONTROL CIRCUIT
U S B CONTROL CIRCUIT
11
A
+5V
+14V
DATA
CLK
+D0
-D0
4
MONITOR
1
B
COMPUTER

FIG. 5

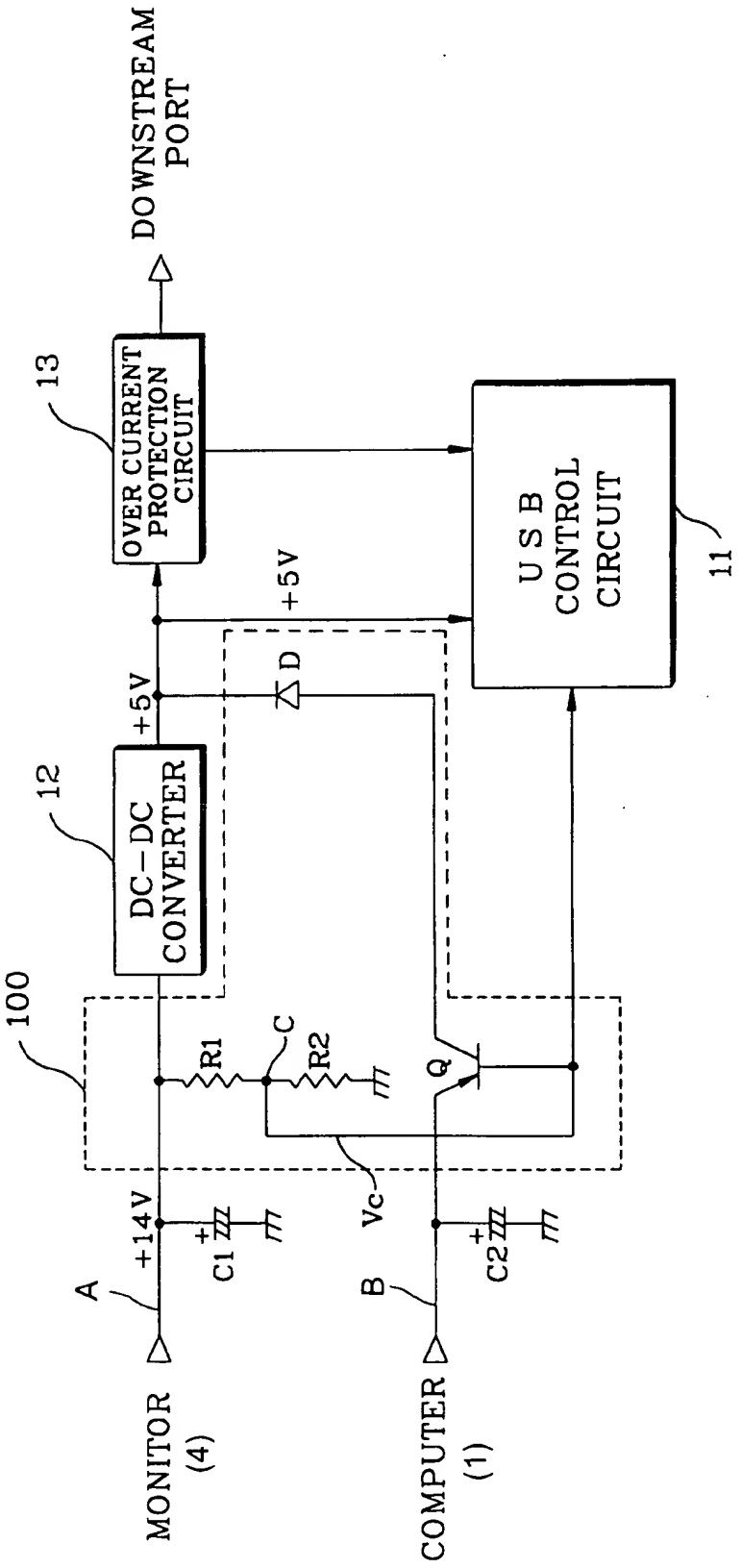
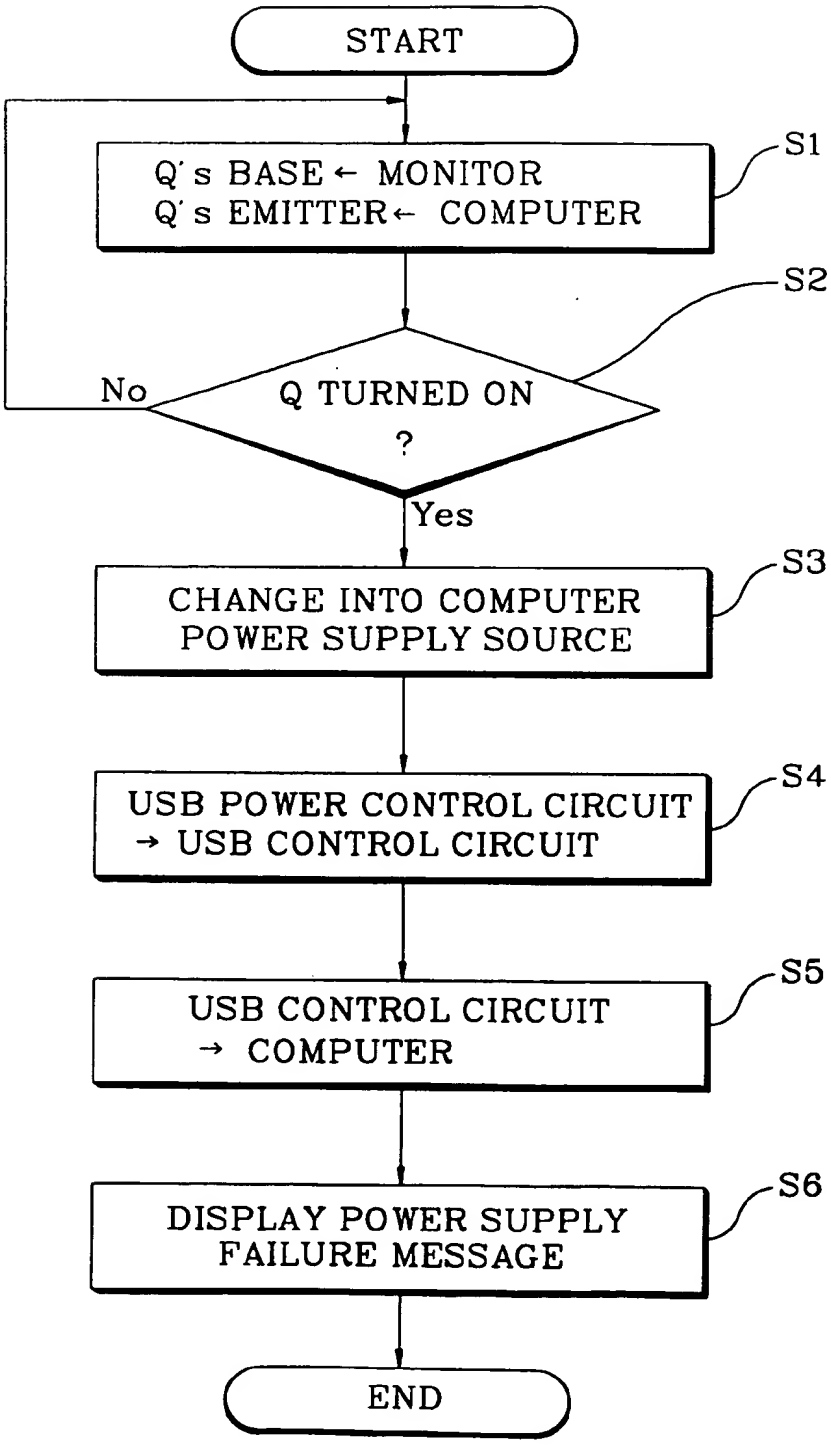

DOWNSTREAM PORT
13
OVER CURRENT PROTECTION CIRCUIT
+5V
D
+5V
12
DC-DC CONVERTER
U S B CONTROL CIRCUIT
11
100
R1
C
R2
Q
+14V
C1
Vc
C2
A
B
MONITOR (4)
COMPUTER (1)

FIG. 6


START
Q's BASE ← MONITOR
Q's EMITTER← COMPUTER
S1
S2
No
Q TURNED ON ?
Yes
CHANGE INTO COMPUTER POWER SUPPLY SOURCE
S3
USB POWER CONTROL CIRCUIT → USB CONTROL CIRCUIT
S4
USB CONTROL CIRCUIT → COMPUTER
S5
DISPLAY POWER SUPPLY FAILURE MESSAGE
S6
END

# POWER CONTROL DEVICE AND METHOD FOR USB

## CLAIM OF PRIORITY

This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C §119 from an application for *Power Control Device And Method For USB* earlier filed in the Korean Industrial Property Office on the 12th day of March 1997, and there duly assigned Serial No. 97-8312, a copy of which is annexed hereto.

## BACKGROUND OF THE INVENTION

1. Technical Field

The present invention relates to a power control device and method for a universal serial bus (USB) in a computer system, and more particularly to a power control device and method for controlling power supplied to a universal serial bus which is connected to a display and a computer system. More specifically, the present invention relates to a power control device and method for controlling the source of power supplied to a universal serial bus where, under normal operating conditions, power is supplied from a display device to a universal serial bus, and, when there is a failure or abnormality in the power supplied from the display device to the universal serial bus, power is supplied from a computer to the universal serial bus.

2. Related Art

A typical personal computer has peripheral devices connected, such as a monitor and keyboard. A user might want to use additional peripheral devices, such as a mouse, printer, light pen, or plotter. When a user tries to use multiple peripheral devices with a computer, it can be difficult to connect them since each peripheral typically has a unique type of connector. The user must carefully match the plug from each peripheral with a corresponding connector on the computer due to all the different connector types. Also, it can be difficult to configure the computer to communicate with all the peripheral devices due to the fact that some peripheral devices require unique types of hardware and software. The task of adding peripheral devices to a computer can be especially arduous for computers that do not support plug-and-play.

To solve the above described problems, a universal serial bus (USB) system has been developed. The universal serial bus is a basic system for connecting peripheral devices to a computer. Peripheral devices connected to a universal serial bus system are also referred to as universal serial bus peripheral devices.

A keyboard or monitor can be directly connected to a computer or a universal serial bus within the computer. Other peripheral devices can be easily connected to the computer with the use of an expanded hub built into the keyboard or monitor, or even via an independent universal serial bus. The expanded hub offers additional connection sockets, and can be connected in a hierarchical tree form. Peripheral devices may be located close to each other or can be located several meters from each other, with the use of a universal serial bus hub.

A universal serial bus is able to connect a total of 127 devices to one computer. The operating voltage transmitted through the universal serial bus is limited to 5 volts. Thus, peripherals connected on a universal serial bus are limited in the amount of power they can consume. A rapid data transmission rate of 12 megabits per second on the universal serial bus is one of the advantageous features of the universal serial bus.



The major advantages of the universal serial bus include the simplicity and convenience of attaching and detaching peripheral devices to the computer. The universal serial bus detects whether a device is added or removed when related information is offered from a computer. This operation is available while the power is ON, unlike existing built-in slots, eliminating the system reboot.

Some examples of universal serial bus systems are disclosed in U.S. Pat. No. 5,621,901 for *Method and Apparatus for Serial Bus Elements of an Hierarchical Serial Bus Assembly to Electrically Represent Data and Control States to Each Other* issued to Morriss et al., U.S. Pat. No. 5,623,610 for *System for Assigning Geographical Addresses in a Hierarchical Serial Bus byEnabling Upstream Port and Selectively Enabling Disabled Ports at Power On/Reset* issued to Knoll et al., and U.S. Pat. No. 5,675,813 for *System and Method for Power Control in a Universal Serial Bus* issued to Holmdahl.

Some examples of power control devices and methods are disclosed in U.S. Pat. No. 5,559,376 for *Power Supply Control System Comprising a Plurality of Power Supply Units* issued to Tachikawa, U.S. Pat. No. 5,486,726 for *Power Supply Control System of Peripheral Equipment of Computer* issued to Kim et al, U.S. Pat. No. 5,404,542 for *Power Line Switching Circuit with Monitor* issued to Cheung, U.S. Pat. No. 5,163,124 for *Method and Apparatus for Controlling Power to Device in a Computer System* issued to Yabe et al., U.S. Pat. No. 5,596,757 for *System and Method for Selectively Providing Termination Power to a SCSI Bus Terminator from a Host Device* issued to Smith, U.S. Pat. No. 5,550,985 for *Special Purpose Computer for Demonstrating Peripheral Devices such as Printers in Which Power is Withdrawn from the Port Connection of the Peripheral Device* issued to Miller et al., and U.S. Pat. No. 5,664,089 for *Multiple Power Domain Power Loss Detection and Interface Disable* issued to Byers et al.

Although presently there do exist systems which partially control the power supplied to a universal serial bus, I have discovered that it would be desirable to further enhance the power control of a universal serial bus to enable it to have a secondary source of power in the event that a primary source of power fails.

## SUMMARY OF THE INVENTION

Accordingly, it is therefore an object of the present invention to provide a universal serial bus power control device and method for a computer system, which, when the power is not supplied to the universal serial bus due to a monitor's power failure, detects this and converts the power offered from the computer into the power supply of the universal serial bus.

It is another object of the present invention to provide a control device and method for displaying a message of power supply failure through a display when there is a trouble in power supply from the monitor.

To accomplish the objects of the present invention, there is provided a universal serial bus (USB) power control device including a universal serial bus control circuit for controlling mutual information transmitted between a computer and its peripheral devices, using data and clocking signals transmitted from a display, a DC—DC converter for processing a power supplied from the display in order to provide an operation power to the universal serial bus control circuit and the peripheral devices, and a universal serial bus power control circuit for detecting a power supplied to the DC—DC converter from the display. If there

is a problem with the power supplied from the display to the universal serial bus circuit, the power supplied from the display is replaced by power supplied from the computer.

For another aspect of the present invention, there is provided a method of controlling a power in a universal serial bus control device including confirming whether a power offered from the display is normal or not, changing a power supply source, if a stable power is not supplied, in order to receive an operation power from a computer main body; transmitting to the computer that an output voltage from the display to the universal serial bus is not normal, and indicating a power supply failure message on the display.

The present invention is more specifically described in the following paragraphs by reference to the drawings attached only by way of example.

## BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the present invention, and many of the attendant advantages thereof, will become readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

FIG. **1** is a block diagram illustrating a conventional computer system;

FIG. **2** is a block diagram illustrating a conventional computer system utilizing a conventional universal serial bus;

FIG. **3** is a block diagram illustrating the universal serial bus shown in FIG. **2**;

FIG. **4** is a block diagram illustrating a universal serial bus, according to the principles of the present invention;

FIG. **5** is a circuit diagram illustrating the universal serial bus shown in FIG. **4**, according to the principles of the present invention; and

FIG. **6** is a flow chart illustrating a power control method of a universal serial bus, according to the principles of the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Refer now to the drawings and particularly to FIG. **1**, which is a block diagram illustrating a conventional computer system. For input means for inputting information into computer main body **1**, there are included a keyboard **2** with multiple keys, and a mouse **3** useful for graphics. As output means, a monitor **4** is used to display information transmitted from the computer main body **1** on a screen.

Refer now to FIG. **2**, which is a block diagram illustrating a conventional computer system utilizing a conventional universal serial bus. Including universal serial bus **10**, there are provided computer main body **1**, monitor **4**, and peripheral devices such as printer **5**, scanner **6** and external modem **7**.

Refer now to FIG. **3**, which is a block diagram illustrating the universal serial bus shown in FIG. **2**. Universal serial bus **10** includes a universal serial bus control circuit **11** for controlling mutual information transmitted between computer **1** and its peripheral devices using data and clocking signals transmitted from monitor **4**, a DC—DC converter **12** for processing the power supplied from monitor **4** and thus providing an operation power to down stream ports **14**, **15** and **16** connected to universal serial bus control circuit **11** and peripheral devices **5**, **6**, and **7**, and an overcurrent protection circuit **13** for detecting the output current of DC—DC converter **12** in order to avoid damage caused due to overcurrent.

For the operational power of 5 volts for the universal serial bus control circuit **11**, the monitor power of 14 V is supplied and DC—DC converter **12** is used. Here, monitor **4** and universal serial bus control circuit **11** are constructed to exchange their data and clocking signals. The power which is stepped down from 14 volts to 5 volts through the DC—DC converter **12** is supplied to universal serial bus control circuit **11** and peripheral devices **5**, **6** and **7** via downstream ports **14**, **15**, and **16**. The computer is connected to the upstream port of universal serial bus **10**. The universal serial bus is supported by the computer **1**.

When computer peripheral devices **5**, **6**, and **7** are connected to downstream ports **14**, **15** and **16** of universal serial bus **10**, computer **1** confirms the registered ID, and if there are no problems, the installation is automatically performed. This allows the user to utilize the peripheral devices without needing to perform any tasks other than plugging in the peripheral devices.

If the 14 volt power from the display is not supplied to the universal serial bus **10**, the universal serial bus control circuit **11** does not operate, and thus all the advantages associated with the universal serial bus will be unavailable. When the universal serial bus control circuit does not operate, the self-diagnosis function is difficult to perform. Above all, the mutual information is not transmitted between the computer and its peripheral devices, making the user uneasy. Further, the source of the problem will not be immediately known to the user. The user may believe that the problem is due to a failure of the DC—DC converter, or the power source of the universal serial bus **10**, or the peripheral devices, because it is difficult for the user to inspect and verify problems in power a supply.

Refer now to FIG. **4**, which is a block diagram illustrating a universal serial bus, according to the principles of the present invention. FIGS. **3** and **4** illustrate some of the same components, which are indicated by the same reference numerals.

In FIG. **4**, the universal serial bus **10** of the present invention includes a universal serial bus power control circuit **100** which detects the power supplied to DC—DC converter **12** from monitor **4**. If there is any problem with the voltage supplied from monitor **4**, the universal power control circuit **100** allows the power supplied from computer **1** to be sent to universal serial bus control circuit **11**.

The universal serial bus power control circuit **100** has a power supply line A from monitor **4** and a power supply line B from computer **1**. The output result is provided to universal serial bus control circuit **11**, and to respective downstream ports **14**, **15**, and **16** for transmission to the peripheral devices via overcurrent protection circuit **13**.

Refer now to FIG. **5**, which is a circuit diagram illustrating the universal serial bus shown in FIG. **4**, according to the principles of the present invention. In FIG. **5**, the universal serial bus control circuit **100** is shown as having resistors R1 and R2, a transistor Q, and a diode D. Detection resistors R1 and R2 are connected to power supply line A supplying 14 volt power to DC—DC converter **12** from monitor **4**. The voltage $V_C$ divided by the two resistors is applied to the base of transistor Q. Power supply line B supplies 5 volt power to the emitter of transistor Q from computer **1**. Diode D is connected between the collector of transistor Q and the output port of DC—DC converter **12**. A signal transmitted to

the universal serial bus control circuit 11 via the base of the transistor Q indicates the current status of the power supplied on power supply line A from the monitor 4.

The voltage supplied to the base of transistor Q from the monitor 4 is detected by resistors R1 and R2. The voltage $V_C$ of the node C between the two resistors is determined by the magnitude of the two resistors. The voltage $V_A$ is the voltage of the power supply line A from the monitor 4. The equation for the voltage $V_C$ is as follows:

$$V_C = \frac{R2}{(R1 + R2)} \times V_A$$

Thus, the voltage $V_C$ applied to the base of transistor Q can be controlled by controlling the values of resistors R1 and R2.

The transistor Q is turned on or off according to the magnitude of the voltage of the power supplied to the emitter of transistor Q from the computer 1 and the magnitude of the voltage of the power supplied to the base of transistor Q from the monitor 4.

If the voltage supplied from the monitor 4 is normal, then the voltage Vc divided and detected by resistors R1 and R2 appears to be 5 volts, and is supplied to the base. The voltage of 5 volts applied to the emitter from computer 1 is equal to that applied to the base, and thus the transistor Q is turned off. The signal transmitted to universal serial bus control circuit 11 via the base indicates the current status of the power supplied from the monitor. Thus, the universal serial bus control circuit 11 receives a signal via the base of transistor Q indicating that the status of the power supplied from the monitor 4 is normal. Through this procedure, the voltage supplied from the monitor 4 is supplied to overcurrent protection circuit 13 and universal serial bus control circuit 11 via DC—DC converter 12.

If the voltage supplied from the monitor 4 is not normal, the operation is as follows. The voltage Vc divided and detected by resistors R1 and R2 becomes below 5 volts. A voltage difference ($V_{BC}$>0.7) is produced between the base and emitter of transistor Q. Thus, the transistor Q is turned on. As a result, the power provided from computer 1 is rectified via the collector of transistor Q and diode D, and then sent to overcurrent protection circuit 13 and universal serial bus control circuit 11. The signal transmitted to universal serial bus control circuit 11 via the base indicates the current status of the power supplied from the monitor. Thus, the universal serial bus control circuit 11 receives a signal via the base of transistor Q indicating that the status of the power supplied from the monitor 4 is not normal. The universal serial bus control circuit 11 detects that the status of the power supplied from the monitor 4 is not normal and then transmits the status to computer 1. Thereafter, computer 1 displays the status on the monitor 4, informing the user of the situation.

Refer now to FIG. 6, which is a flow chart illustrating a power control method of a universal serial bus, according to the principles of the present invention. In FIG. 6, the operation of controlling the power of universal serial bus 10 is explained with a flowchart. In step S1, the voltage Vc divided from the voltage supplied from the monitor 4, using resistors R1 and R2, is applied to the base of transistor Q. The power from the computer is supplied to the emitter of transistor Q.

In step S2, the status of the transistor Q is detected. Transistor Q can be either on or off. Using the detected status of transistor Q, it is determined whether a power supply from the monitor 4 is normal or not normal. When the transistor Q is off, the power supply from the monitor 4 on power supply line A is considered to be normal.

The transistor Q is turned on when the power supplied from the monitor 4 on power supply line A is considered to be not normal. Step S3 is performed when the transistor Q is turned on, indicating that the power supplied from the monitor 4 is not normal. When the transistor Q is detected to be turned on, the operational power provided from the computer 1 is output via the collector. Thus, in step S3 the power supply source is changed from the monitor 4 to the computer 1. In step S4, a signal is sent from the universal serial bus power control circuit to universal serial bus control circuit indicating that the power supply from the monitor 4 is not normal.

In step S5, the universal serial bus control circuit transmits a signal to the computer 1 indicating that the power supply from the monitor 4 is not normal. In step S6, a power supply failure message is displayed on the monitor in order to inform the user. The message can be shown using an on-screen display. The information is contained in a memory of the computer system, and the microcomputer transmits it to the on-screen display.

As described above, the present invention is capable of detecting the fact that the power supply to the universal serial bus from the monitor is not normal, and is capable of replacing the power source that is not normal with a power source that is normal. Thus, the monitor supplying abnormal power is replaced by the computer supplying normal power. When the power supplied from the monitor is not normal, a power supply failure message is transmitted from the universal serial bus to the computer. Then the power supply failure message is displayed on the monitor. Thus, the user can stay informed of the status of the power to the universal serial bus.

While there have been illustrated and described what are considered to be preferred embodiments of the present invention, it will be understood by those skilled in the art that various changes and modifications may be made, and equivalents may be substituted for elements thereof without departing from the true scope of the present invention. In addition, many modifications may be made to adapt a particular situation to the teaching of the present invention without departing from the central scope thereof. Therefore, it is intended that the present invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out the present invention, but that the present invention includes all embodiments falling within the scope of the appended claims.

What is claimed is:

1. A universal serial bus power control apparatus, comprising:

a control circuit controlling a transmission of data in a universal serial bus hub;

a converter unit receiving a first input power from a video display, and outputting a first output power corresponding to the first input power to at least one output port; and

a power controller detecting the first input power received by said converter unit from the video display, said power controller receiving a second input power from a processing unit;

when said power controller detects that the first input power is abnormal, said power controller outputting a second output power corresponding to the second input power to the at least one output port.

2. The power control apparatus of claim 1, wherein said control circuit controls the transmission of data between the video display and the at least one output port.

3. The power control apparatus of claim 1, wherein said power controller comprises a transistor having a control electrode receiving the first input power from the video display, a first electrode of a principal electrically conducting channel receiving the second input power from the processing unit, and a second electrode of the principal electrically conducting channel coupled electrically to the at least one output port.

4. The power control apparatus of claim 3, wherein said power controller further comprises a diode rectifying the second input power, said diode having an anode connected to said transistor and a cathode coupled electrically to the at least one output port.

5. The power control apparatus of claim 1, wherein said control circuit outputs a control signal when the first input power is abnormal, and the video display displays a message in response to the control signal informing the user that the first input power received from the video display is abnormal.

6. A universal serial bus power control apparatus, comprising:

a video display conveying varying visual information to a user, and supplying a first power;

a processing unit connected to said video display, processing data signals and the visual information, and supplying a second power;

a plurality of peripheral units connected to said video display and said processing unit, providing supplementary functions to said processing unit, receiving the data signals, and selectively receiving one of the first and second powers; and

a control unit receiving the data signals, controlling a transmission of the data signals to said processing unit and said plurality of peripheral units, receiving the first power from said video display and the second power from said processing unit, detecting the first power, and supplying the second power to said plurality of peripheral units according to the first power, the first power being a voltage selected from the group consisting of a plurality of standard voltages and a plurality of nonstandard voltages.

7. The power control apparatus of claim 6, wherein said control unit supplies the second power to said plurality of peripheral units when the first power corresponds to the plurality of nonstandard voltages.

8. The power control apparatus of claim 6, wherein said control unit does not supply the second power to said plurality of peripheral units when the first power corresponds to the plurality of standard voltages.

9. A universal serial bus power control apparatus, comprising:

a converter unit receiving a first power from a video display, the video display conveying varying visual information to a user;

a power controller detecting the first power, wherein the first power is a voltage selected from the group consisting of a plurality of standard voltages and a plurality of nonstandard voltages, said power controller receiving a second power from a processing unit connected to the video display, the processing unit processing data signals and the visual information;

when the voltage of the first power corresponds to the plurality of standard voltages, said converter unit transmits the first power to at least one output port;

when the voltage of the first power corresponds to the plurality of nonstandard voltages, said power controller transmits the second power to the at least one output port; and

a control circuit controlling data signals transmitted between the processing unit and the at least one output port, said control circuit transmitting a control signal to the video display to inform the user of the nonstandard voltage of the first power when the voltage of the first power corresponds to the plurality of nonstandard voltages.

10. The power control apparatus of claim 9, wherein said power controller comprises:

a divider converting the first power to an intermediate power;

a detector detecting the intermediate power; and

a rectifier rectifying the second power according to the intermediate power.

11. The power control apparatus of claim 10, wherein said divider comprises a plurality of resistors converting the first power to the intermediate power.

12. The power control apparatus of claim 10, wherein said detector comprises a transistor having a control electrode receiving the intermediate power from said divider, a first electrode of a principal electrically conducting channel receiving the second power from the processing unit, and a second electrode of the principal electrically conducting channel connected to said rectifier.

13. The power control apparatus of claim 10, wherein said rectifier comprises a diode having an anode connected to said detector and a cathode coupled electrically to the at least one output port.

14. The power control apparatus of claim 9, wherein said converter unit steps down the voltage of the first power received from the video display, and then outputs the stepped down first power to the at least one output port.

15. A universal serial bus power control apparatus, comprising:

a video display conveying varying visual information to a user, transmitting data signals and clock signals, and supplying a first power;

a processing unit connected to said video display, processing the data signals and the visual information, and supplying a second power;

a plurality of peripheral units connected to said video display and said processing unit, providing supplementary functions to said processing unit, and receiving the data signals;

a first control unit receiving the data and clock signals from said video display, and controlling a transmission of the data signals to said processing unit and said plurality of peripheral units according to the clock signals;

a second control unit receiving the first power from said video display and the second power from said processing unit, converting the first power to a third power, detecting the third power, and supplying the second power to said first control unit and said plurality of peripheral units according to the third power; and

a power unit receiving the first power from said video display, converting the first power to a fourth power, and transmitting the fourth power to said first control unit and plurality of peripheral units, the third power being a voltage selected from the group consisting of a plurality of standard voltages and a plurality of nonstandard voltages.

16. The power control apparatus of claim 15, wherein said second control unit rectifies the second power when the third power corresponds to the plurality of nonstandard voltages, and said second control unit supplies the second power to

said first control unit and said plurality of peripheral units when the third power corresponds to the plurality of nonstandard voltages.

17. The power control apparatus of claim 15, wherein said second control unit does not rectify the second power when the third power corresponds to the plurality of standard voltages, said second control unit does not supply the second power to said first control unit when the third power corresponds to the plurality of standard voltages, and said second control unit does not supply the second power to said plurality of peripheral units when the third power corresponds to the plurality of standard voltages.

18. A method of controlling power in a universal serial bus power control apparatus, comprising the steps of:

receiving a first power from a video display, said video display conveying varying visual information to a user;

detecting the first power, wherein the first power is a voltage selected from the group consisting of a plurality of standard voltages and a plurality of nonstandard voltages;

receiving a second power from a processing unit connected to said video display, said processing unit processing data signals and the visual information;

when the voltage of the first power corresponds to the plurality of standard voltages, transmitting the first power from a control unit to a plurality of peripheral units, said plurality of peripheral units providing supplementary functions to said processing unit and connected to said video display and said processing unit;

when the voltage of the first power corresponds to the plurality of nonstandard voltages, transmitting the second power from said control unit to the plurality of peripheral units; and

transmitting a control signal from said control unit to said video display informing the user of the voltage of the first power.

19. The method of claim 18, wherein said control unit comprises a controller detecting the voltage of the first power, and then transmitting to said plurality of peripheral units a primary power selected from among the first and second powers.

20. The method of claim 18, wherein said control unit comprises a transistor having a control electrode receiving the first power from said video display, a first electrode of a principal electrically conducting channel receiving the second power from said processing unit, and a second electrode of the principal electrically conducting channel connected to said plurality of peripheral units.

* * * * *

US006128743A

# United States Patent [19]

Rothenbaum

[11] Patent Number: 6,128,743

[45] Date of Patent: Oct. 3, 2000

[54] **INTELLIGENT SYSTEM AND METHOD FOR UNIVERSAL BUS COMMUNICATION AND POWER**

[75] Inventor: **Perry Rothenbaum**, Barrington, Ill.

[73] Assignee: **Pertech, Inc.**, Barrington, Ill.

[21] Appl. No.: **09/162,047**

[22] Filed: **Sep. 28, 1998**

[51] **Int. Cl.**[7] ..... **G06F 1/26**

[52] **U.S. Cl.** ..... **713/300**; 710/100

[58] **Field of Search** ..... 713/300, 310, 713/320, 330; 710/102, 104, 129, 63, 2, 8, 100; 709/220; 370/386; 323/231; 714/14; 361/686

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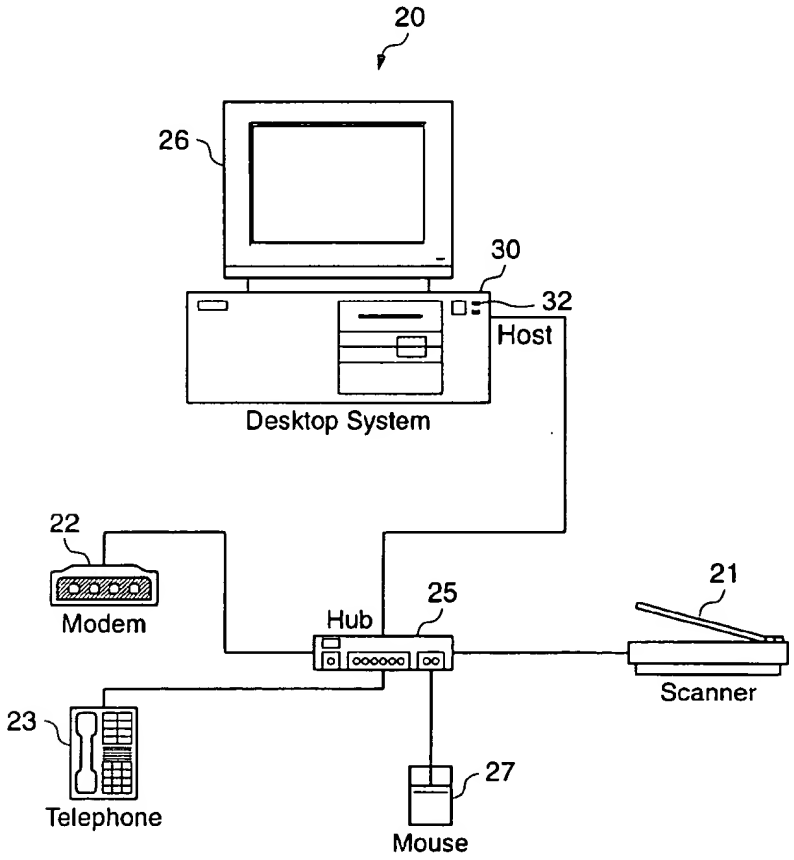
*Primary Examiner*—Gopal C. Ray

*Attorney, Agent, or Firm*—Skjerven Morrill MacPherson LLP; Ken J. Koestner; Margaret M. Kelton

[57] **ABSTRACT**

A bus hub for connection via a serial bus to a serial bus host hub includes a connector to a power supply, a bus controller and a switch coupled to the bus controller and to the power supply. The switch switches the bus hub between being powered by the power supply and being powered by the power from the serial bus host hub by switching the mode of operation between self-powered mode and bus-powered mode. A system for controlling communication and power in a serial bus includes a serial bus hub for detachably coupling at least one peripheral to a computer system, and a serial bus host hub capable of delivering power to the serial bus hub. The system also includes a power supply coupled to the serial bus hub that delivers power to the serial bus hub. The system also includes a bus controller that receives signals from the computer system through the serial bus, and receiving signals from the serial bus hub. The system also includes a switch that switches the serial bus hub between being powered by the power supply and being powered by the power from a serial bus host hub.

**31 Claims, 12 Drawing Sheets**



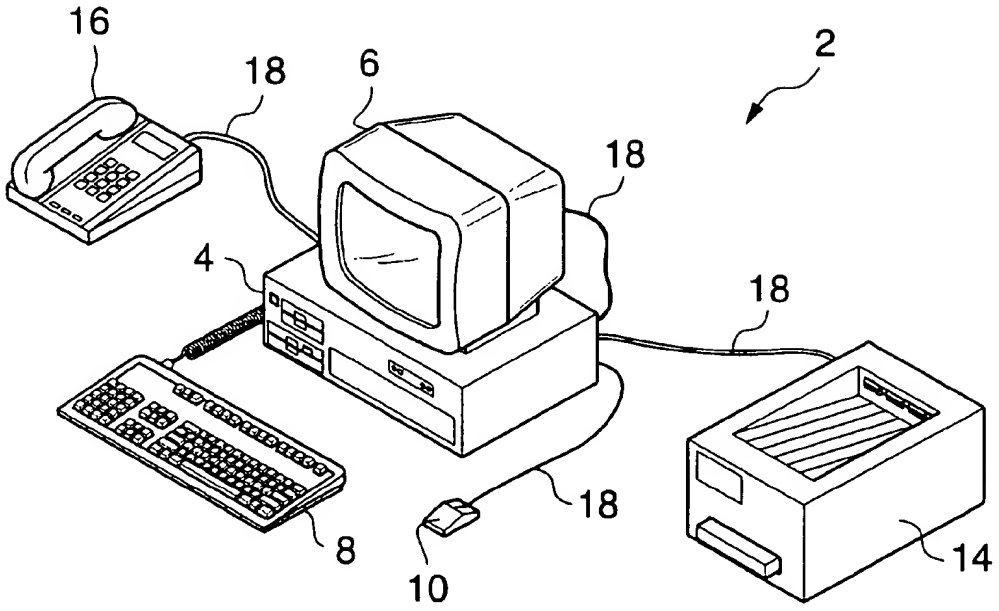



FIG. 1
(PRIOR ART)

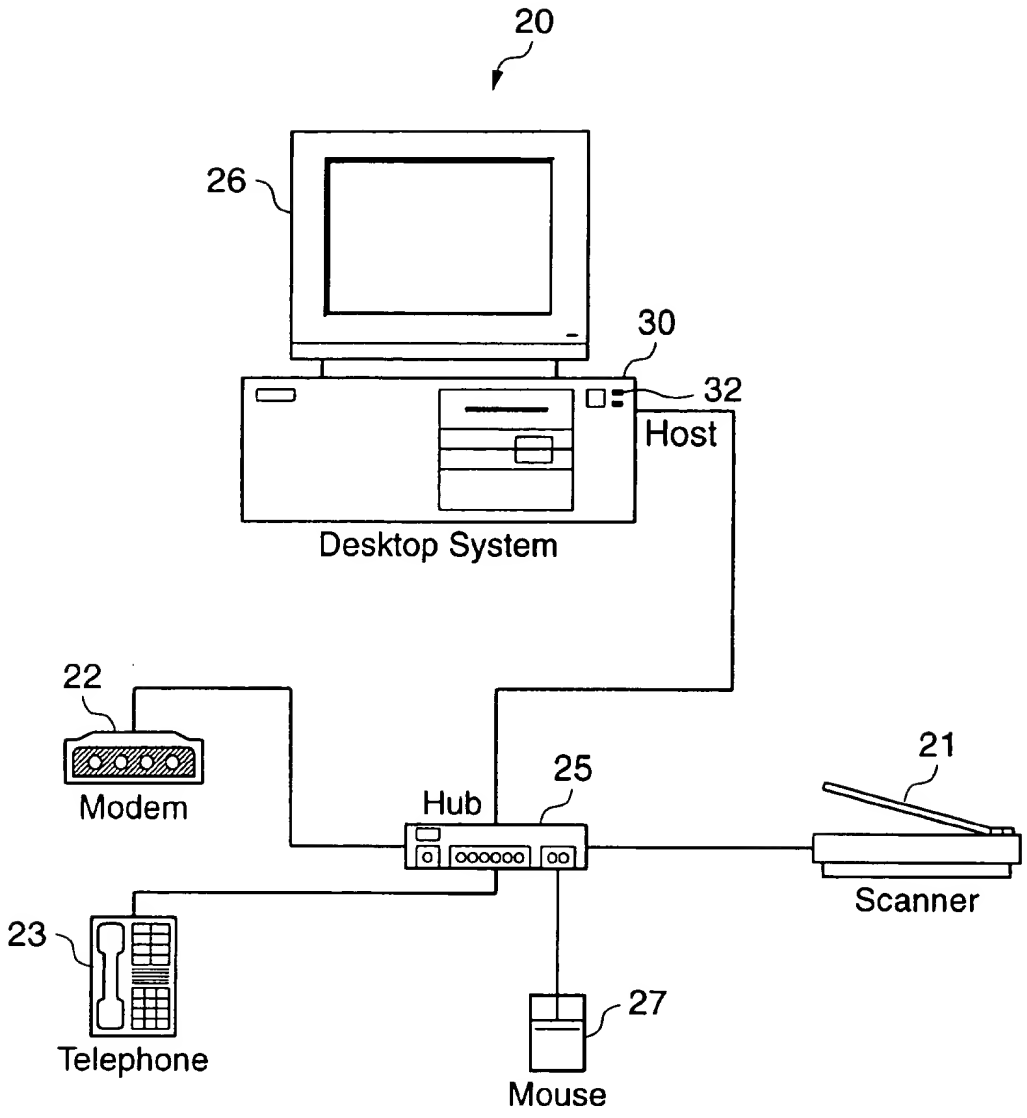

20
26
30
32
Host
Desktop System
22
Modem
25
Hub
21
Scanner
23
Telephone
27
Mouse

FIG. 2

FIG. 3A

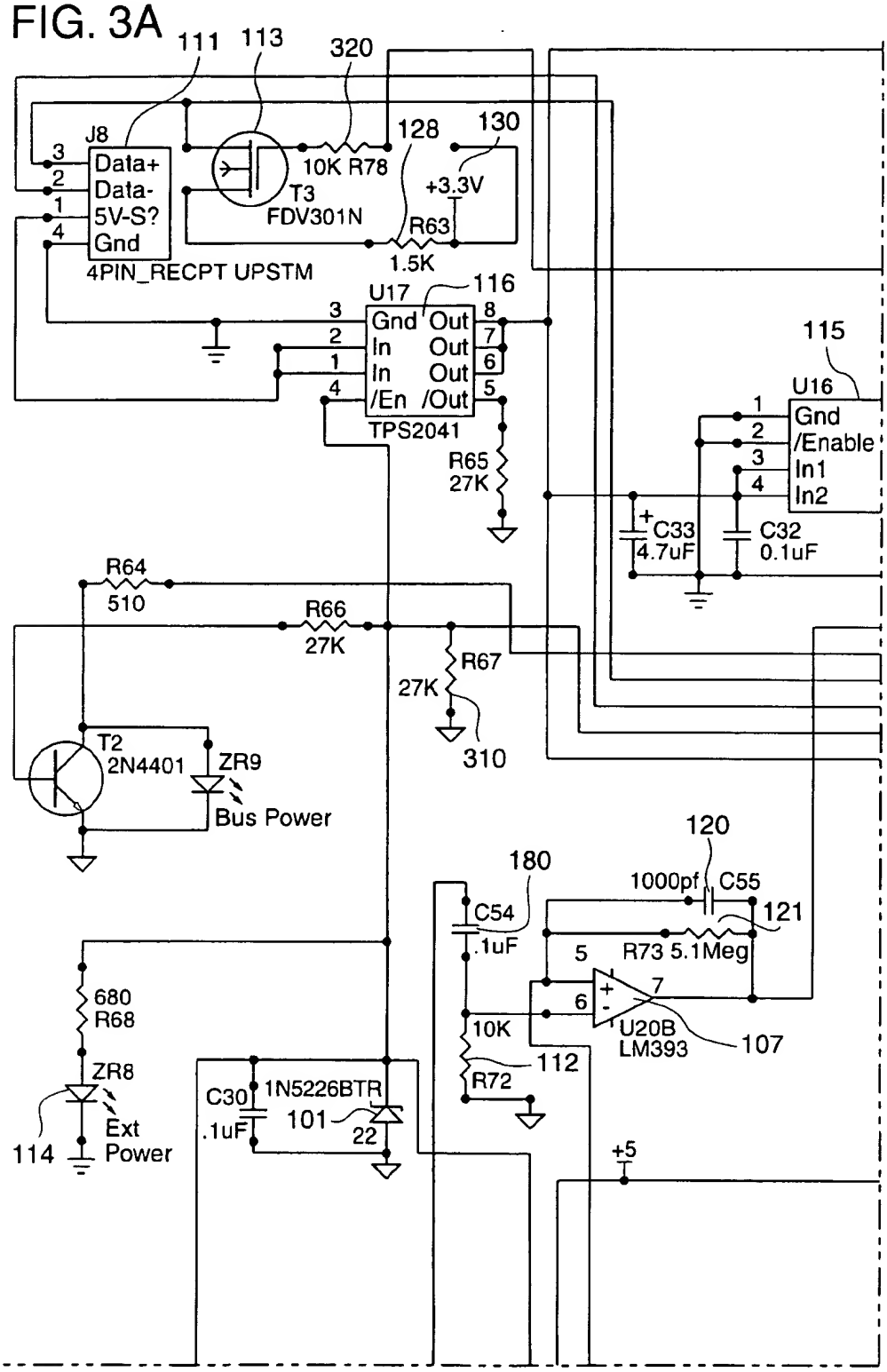

111
113
320
J8
Data+
Data-
5V-S?
Gnd
4PIN_RECPT UPSTM
T3
FDV301N
10K R78
128
130
+3.3V
R63
1.5K
U17
116
Gnd
In
In
/En
Out
Out
Out
/Out
TPS2041
R65
27K
115
U16
Gnd
/Enable
In1
In2
C33
4.7uF
C32
0.1uF
R64
510
R66
27K
R67
27K
310
T2
2N4401
ZR9
Bus Power
120
180
1000pf
C55
C54
.1uF
121
R73 5.1Meg
U20B
LM393
107
10K
R72
112
680
R68
ZR8
Ext
Power
114
C30
.1uF
1N5226BTR
101
22
+5

FIG. 3B

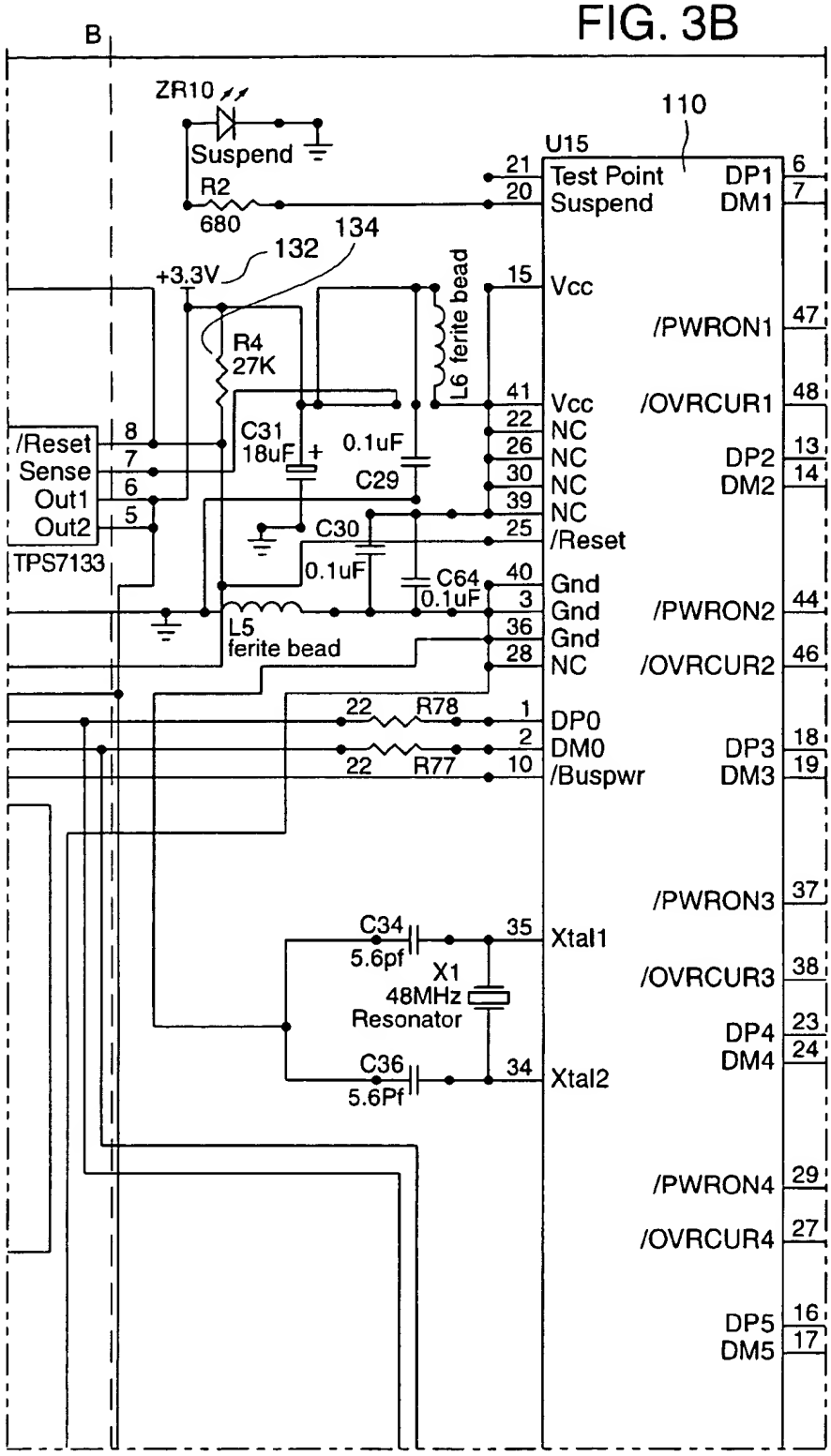
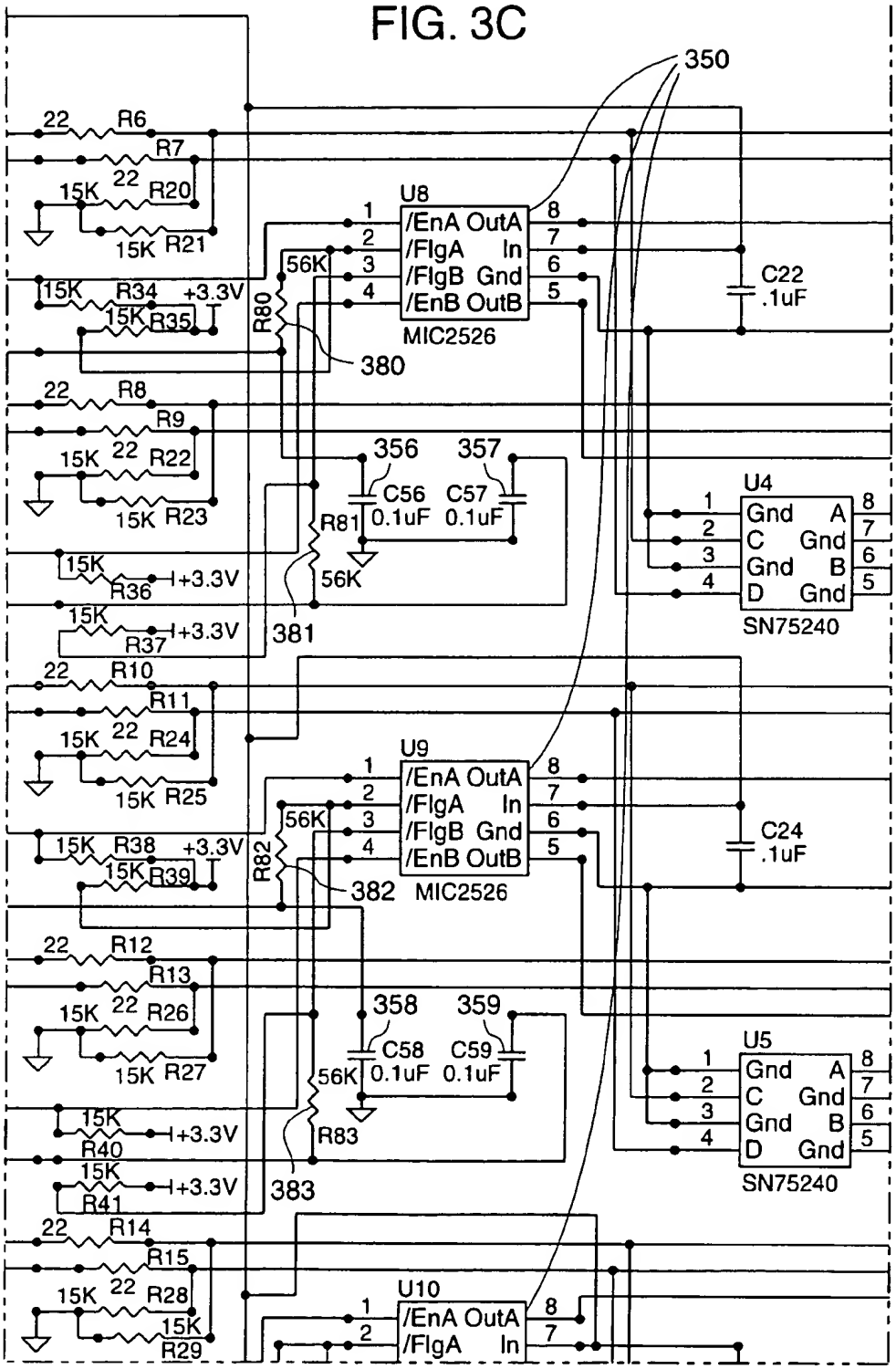

B
ZR10
Suspend
R2
680
110
U15
21 Test Point
20 Suspend
DP1 6
DM1 7
132
134
+3.3V
R4
27K
L6 ferite bead
15 Vcc
/PWRON1 47
41 Vcc
/OVRCUR1 48
22 NC
26 NC
30 NC
39 NC
25 /Reset
DP2 13
DM2 14
/Reset
Sense
Out1
Out2
TPS7133
8
7
6
5
C31
18uF
0.1uF
C29
C30
0.1uF
C64
0.1uF
40 Gnd
3 Gnd
36 Gnd
28 NC
/PWRON2 44
/OVRCUR2 46
L5
ferite bead
22 R78
1 DP0
2 DM0
22 R77
10 /Buspwr
DP3 18
DM3 19
/PWRON3 37
C34
5.6pf
35 Xtal1
X1
48MHz
Resonator
/OVRCUR3 38
DP4 23
DM4 24
C36
5.6Pf
34 Xtal2
/PWRON4 29
/OVRCUR4 27
DP5 16
DM5 17

FIG. 3C


350
U8
/EnA OutA
/FlgA In
/FlgB Gnd
/EnB OutB
MIC2526
U4
Gnd A
C Gnd
Gnd B
D Gnd
SN75240
U9
U5
U10
22 R6
R7
15K 22 R20
15K R21
15K R34 +3.3V
15K R35
56K R80
380
22 R8
R9
15K 22 R22
15K R23
356 357
C56 C57
0.1uF 0.1uF
R81 56K
15K R36 +3.3V
15K R37 +3.3V
381
22 R10
R11
15K 22 R24
15K R25
15K R38 +3.3V
15K R39
56K R82
382
22 R12
R13
15K 22 R26
15K R27
358 359
C58 C59
56K 0.1uF 0.1uF
R83
15K R40 +3.3V
15K R41 +3.3V
383
22 R14
R15
15K 22 R28
15K R29
C22 .1uF
C24 .1uF

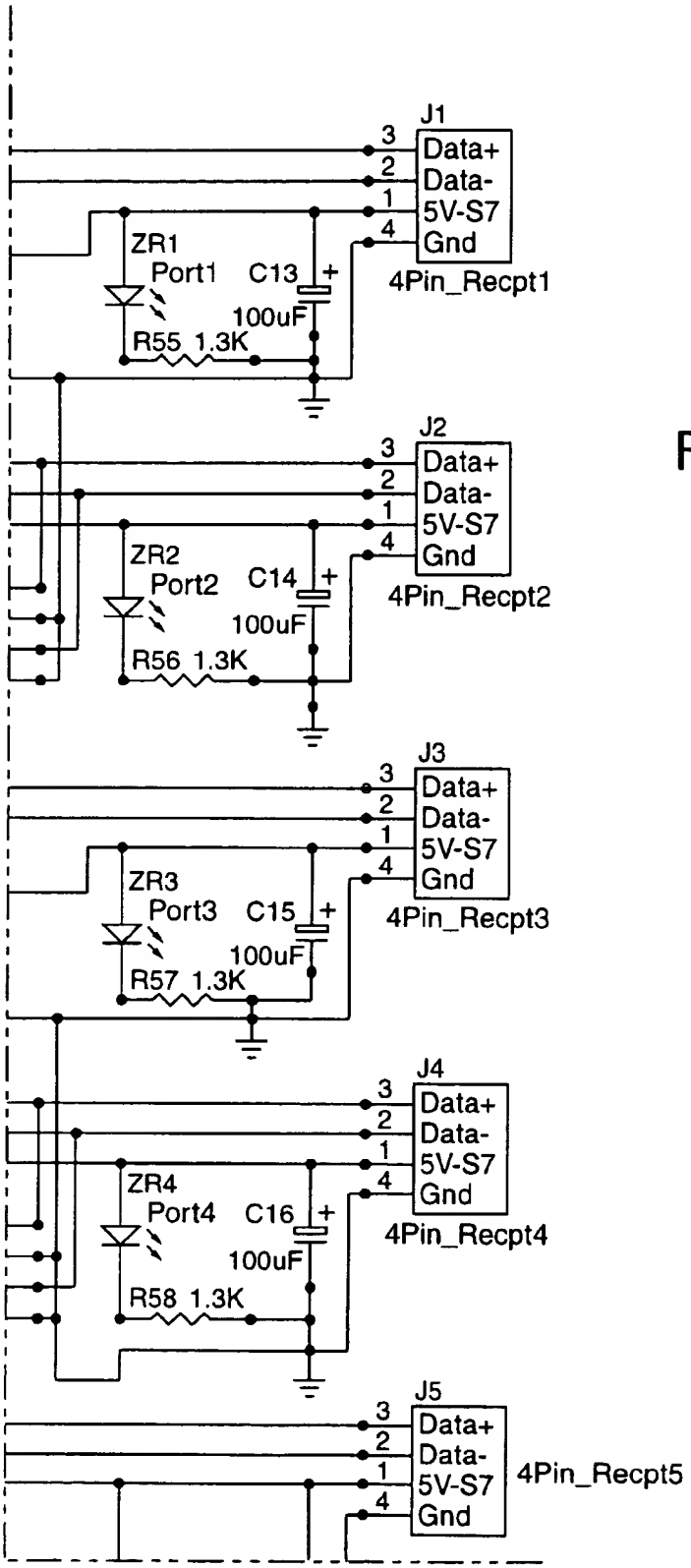

J1
3
2
1
4
Data+
Data-
5V-S7
Gnd
4Pin_Recpt1
ZR1
Port1
C13
100uF
R55 1.3K
J2
4Pin_Recpt2
ZR2
Port2
C14
100uF
R56 1.3K
J3
4Pin_Recpt3
ZR3
Port3
C15
100uF
R57 1.3K
J4
4Pin_Recpt4
ZR4
Port4
C16
100uF
R58 1.3K
J5
4Pin_Recpt5

FIG. 3D

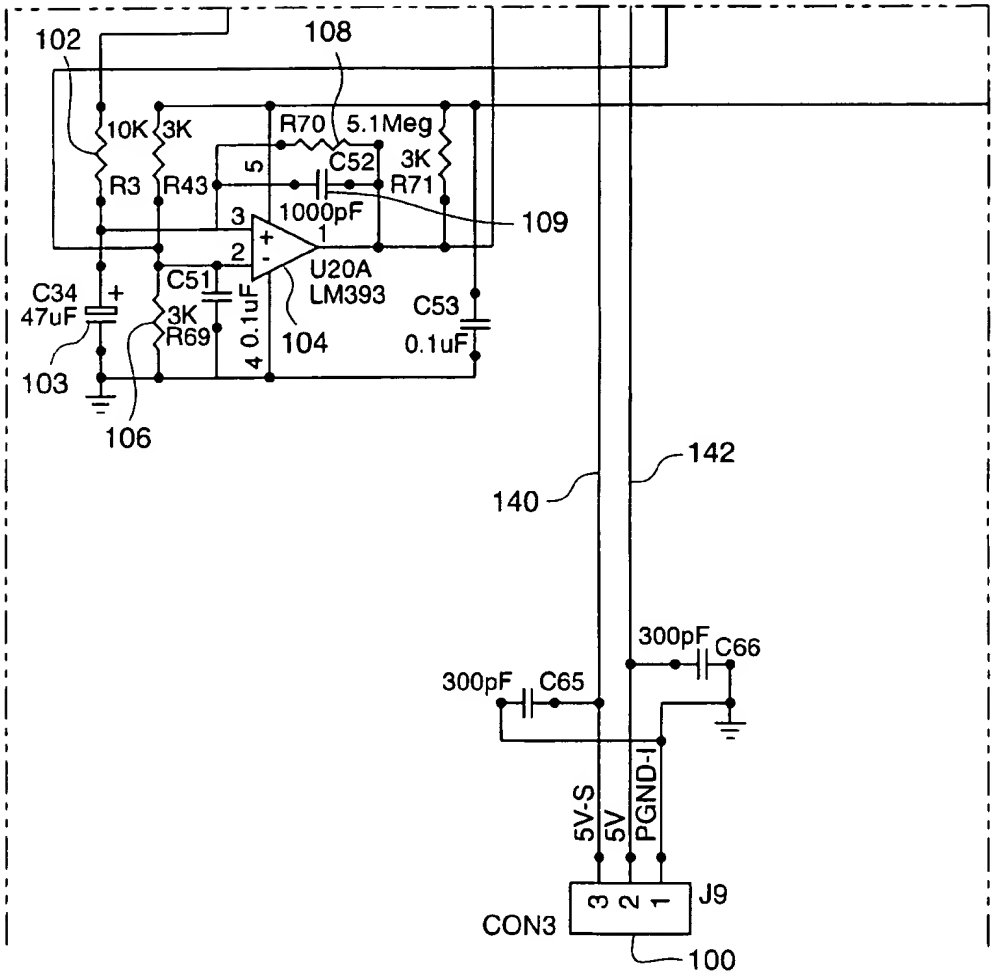

102
108
10K
3K
R70
5.1Meg
C52
3K
R3
R43
R71
1000pF
109
U20A
LM393
104
C34
47uF
C51
0.1uF
3K
R69
C53
0.1uF
103
106
140
142
300pF
C66
300pF
C65
5V-S
5V
PGND-I
3
2
1
J9
CON3
100

FIG. 3E

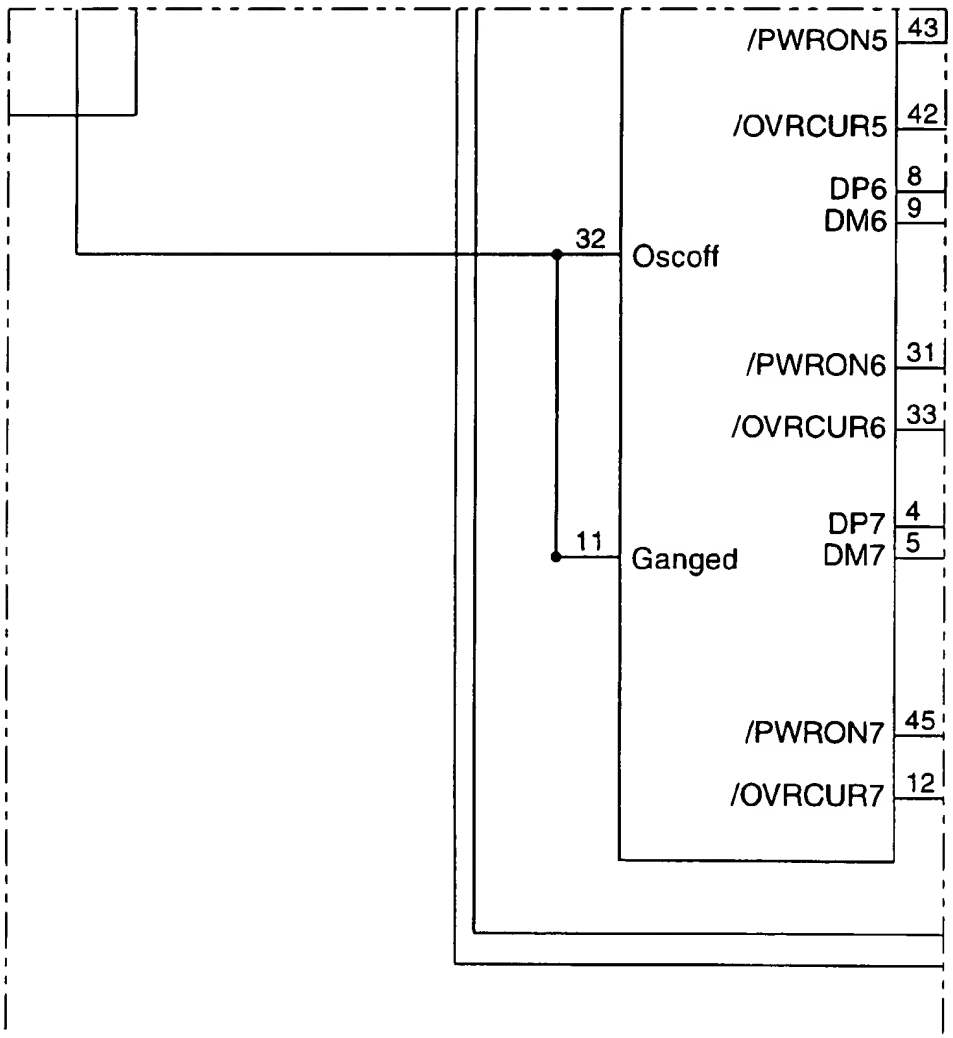

/PWRON5
43
/OVRCUR5
42
DP6
8
DM6
9
32
Oscoff
/PWRON6
31
/OVRCUR6
33
DP7
4
11
Ganged
DM7
5
/PWRON7
45
/OVRCUR7
12

FIG. 3F

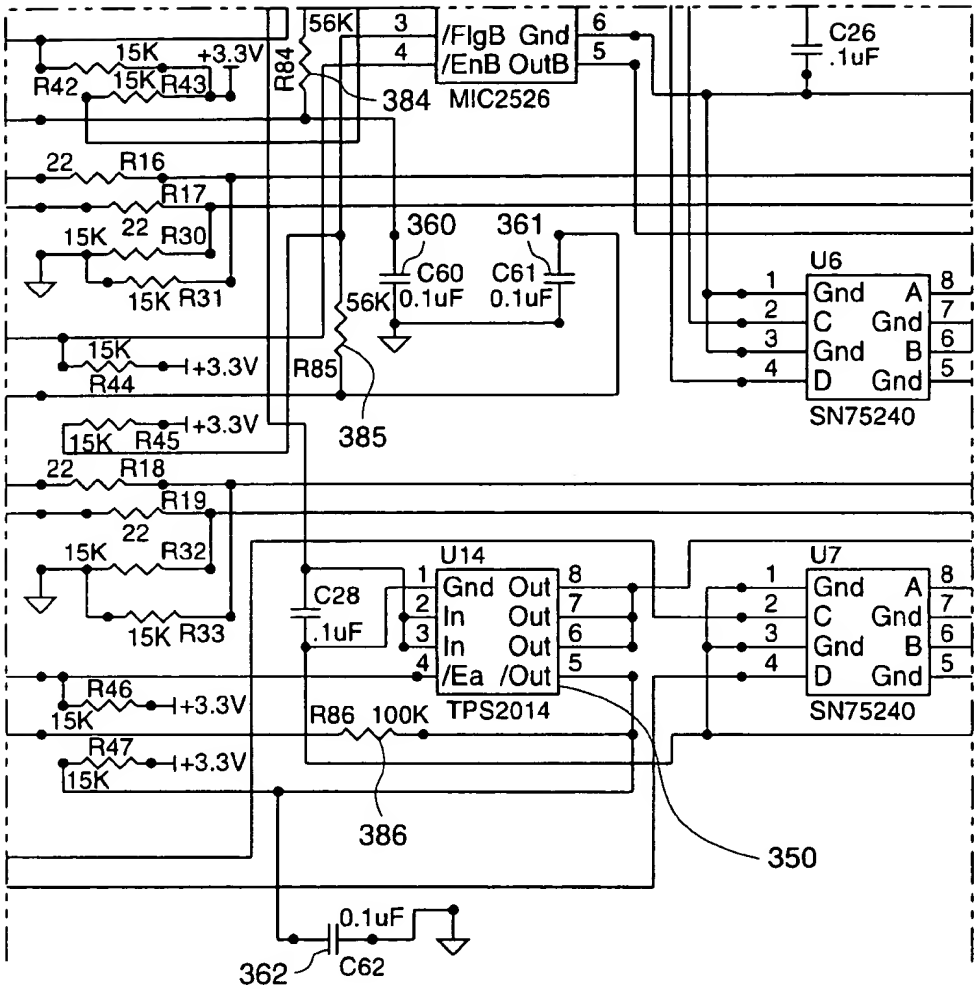

56K
3
4
/FlgB Gnd
/EnB OutB
6
5
MIC2526
384
C26
.1uF
15K
+3.3V
R42
15K
R43
R84
22
R16
R17
15K
22
R30
15K R31
360
361
C60
0.1uF
C61
0.1uF
56K
U6
1
2
3
4
Gnd A
C Gnd
Gnd B
D Gnd
8
7
6
5
SN75240
15K
R44
+3.3V
R85
385
15K R45
+3.3V
22
R18
R19
22
15K
R32
15K R33
U14
C28
.1uF
1
2
3
4
Gnd Out
In Out
In Out
/Ea /Out
8
7
6
5
TPS2014
U7
SN75240
R46
15K
+3.3V
R47
15K
+3.3V
R86 100K
386
350
0.1uF
362
C62

FIG. 3G

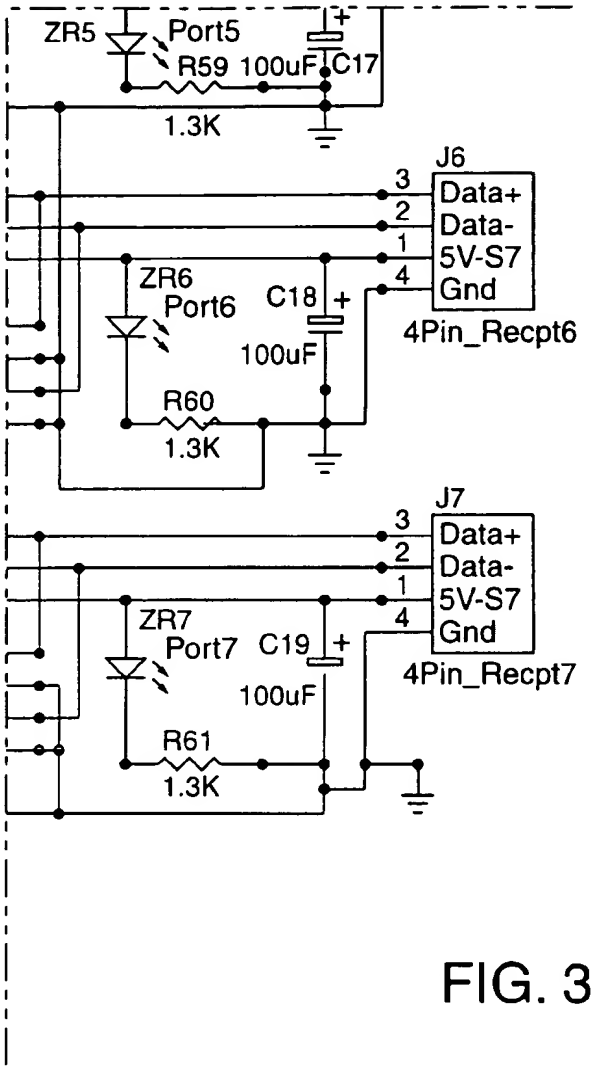



FIG. 3H

| | | | |
|---|---|---|---|
| FIG. 3A | FIG. 3B | FIG. 3C | FIG. 3D |
| FIG. 3E | FIG. 3F | FIG. 3G | FIG. 3H |

FIG. 3

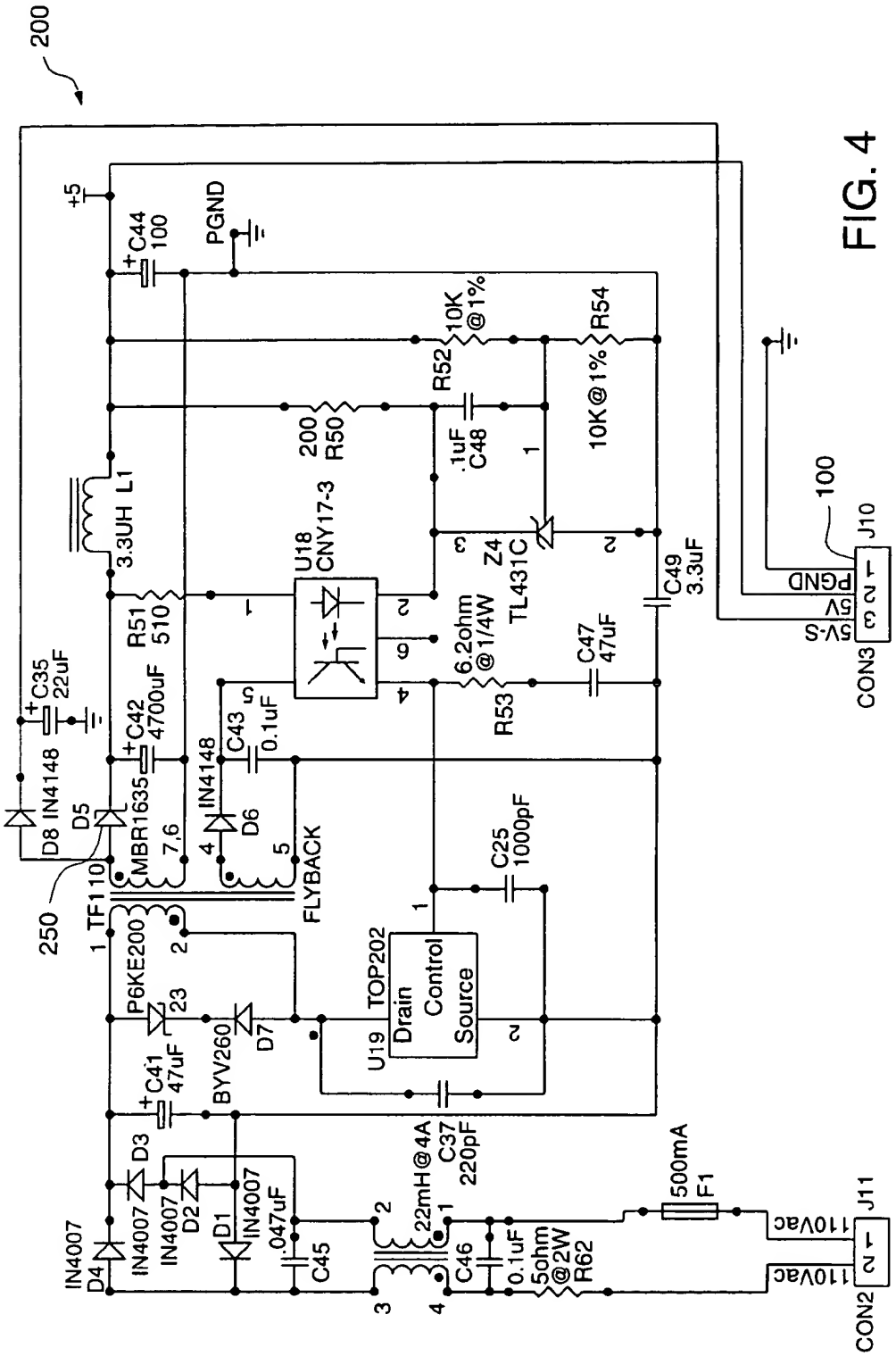

200
+5
PGND
C44 100
10K @1% R52
R54 10K@1%
200 R50
.1uF C48
3.3UH L1
U18 CNY17-3
Z4 TL431C
C49 3.3uF
100
J10
PGND
5V
5V-S
CON3
R51 510
6.2ohm @1/4W R53
C47 47uF
C35 22uF
C42 4700uF
C43 0.1uF
IN4148
D8 IN4148
D5
MBR1635
D6
FLYBACK
C25 1000pF
250
TF1
P6KE200
TOP202
Drain
Control
Source
U19
D7
BYV260
C41 47uF
D3
IN4007
D2
D1
.047uF C45
22mH@4A C37 220pF
500mA F1
C46 0.1uF
5ohm @2W R62
110Vac
110Vac
J11
CON2

FIG. 4

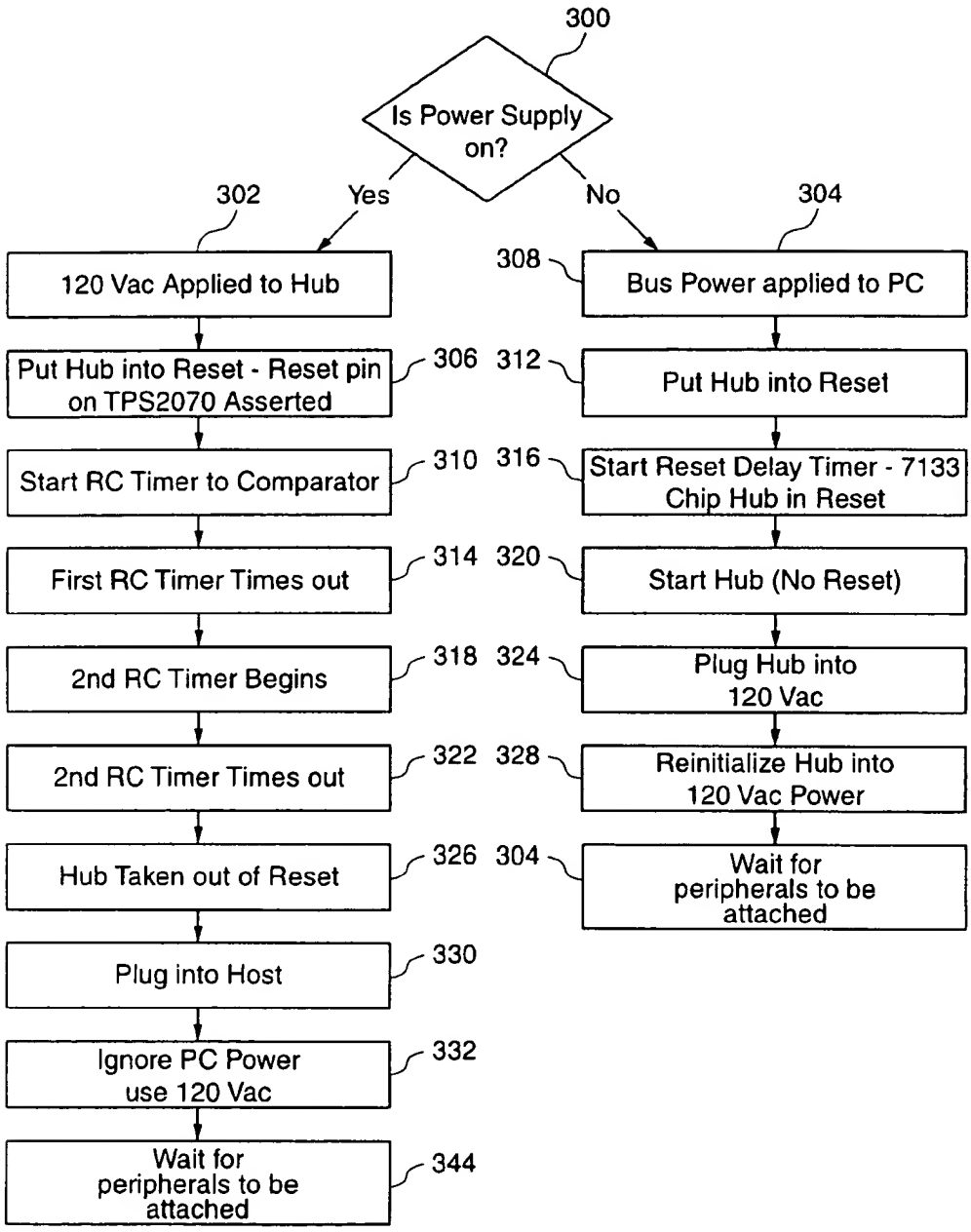

300
Is Power Supply on?
Yes
No
302
304
120 Vac Applied to Hub
308
Bus Power applied to PC
Put Hub into Reset - Reset pin on TPS2070 Asserted
306
312
Put Hub into Reset
Start RC Timer to Comparator
310
316
Start Reset Delay Timer - 7133 Chip Hub in Reset
First RC Timer Times out
314
320
Start Hub (No Reset)
2nd RC Timer Begins
318
324
Plug Hub into 120 Vac
2nd RC Timer Times out
322
328
Reinitialize Hub into 120 Vac Power
Hub Taken out of Reset
326
304
Wait for peripherals to be attached
Plug into Host
330
Ignore PC Power use 120 Vac
332
Wait for peripherals to be attached
344

FIG. 5

# INTELLIGENT SYSTEM AND METHOD FOR UNIVERSAL BUS COMMUNICATION AND POWER

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to serial bus technology and more particularly, to power control and communication in universal serial bus technology.

2. Description of the Related Art

Personal computer systems have attained widespread use. These personal computer systems now provide computing power to many segments of today's society. A personal computer system can usually be defined as a desktop or portable microcomputer that includes a system unit having a system processor with associated volatile and non-volatile memory, a display monitor, a keyboard, a hard disk storage device or other type of storage media such as a floppy disk drive or a compact disk read only memory (CD ROM) drive. One of the distinguishing characteristics of these systems is the use of a system board or motherboard to electrically connect these components together. These personal computer systems are information handling systems which are designed primarily to give independent computing power to a single user or group of users and are inexpensively priced for purchase by individuals or small businesses.

FIG. **1**, which is labeled "prior art", represents a typical computer system **2** including a host computer **4** holding a processor and memory (not shown). The peripherals shown connected to the system **2** include a mouse **10**, a keyboard **8**, a telephone **16** and an external disk drive **14**. Each of these peripherals is connected to the system **2** through a number of different interfaces and connectors, with each peripheral having a separate socket and connector.

Many personal computers hold multiple external peripheral interfaces for attaching peripheral devices. For example, a printer and a modem typically require an RS-232 interface, a peripheral disk drive typically requires a Small Computer System Interface (SCSI), a mouse or a keyboard typically requires a third interface. Thus, multiple interfaces become necessary for a personal computer to operate. With each type of interface comes a different type of connector and a different power requirement.

Alternatively, an external hub could be used to serve as a central location for connecting peripheral devices to the computer using the same type of connector. A hub compatible with the Universal Serial Bus (USB) standard offers a single type of connector. One problem with using a USB hub, however, is that there are several power modes supported by the specification, so-called "bus-powered" and so-called "self-powered" modes.

Therefore, it can be appreciated that there is a need for a universal hub that has the advantages of both "bus-powered" hubs and "self-powered" hubs, but in a single hub that has the capability of controlled switching between power modes.

## SUMMARY OF THE INVENTION

In accordance with an aspect of the present invention, a bus hub for connection via a serial bus to a serial bus host hub includes a connector to a power supply, a bus controller and a switch coupled to the bus controller and to the power supply. The switch switches the bus hub between being powered by the power supply and being powered by the power from the serial bus host hub by switching the mode of operation between self-powered mode and bus-powered mode.



In accordance with another aspect of the present invention, a system for controlling communication and power in a serial bus includes a serial bus hub for detachably coupling peripherals to a computer system. The system also includes a serial bus host hub capable of delivering power to the serial bus hub and a power supply electrically coupled to the serial bus hub that is capable of delivering power to the serial bus hub. The system also includes a bus controller coupled to the hub that receives signals from the computer system through the serial bus and signals from the serial bus hub. the system also includes a switch coupled to the bus controller and to the power supply. The switch switches the serial bus hub between being powered by the power supply and being powered by the power from a serial bus host hub.

In accordance with an aspect of the invention, a method of operating a serial bus hub to control power allocation and communication for detachably coupling a plurality of peripherals to a computer includes a host hub powered by the computer, and the serial bus hub coupled to a power supply. According to this method, the serial bus hub first determines whether it is receiving power from a power supply, and if the serial bus hub is receiving power from a power supply, the serial bus hub initializes to receive power from the power supply. If the serial bus hub does not receive power from the power supply, the serial bus hub initializes to receive power from an upstream serial bus host hub coupled to the serial bus hub. Once initialized, the serial bus hub supplies power to any peripherals coupled to the hub.

Many advantages are achieved by the described serial bus hub, system and method. One advantage is that the described hub, system and method provide automatic switching and reduced complexity by signaling an upstream host of a switch through a single data line instead of the entire input line received on the serial bus. Another advantage of the described serial bus hub system and method is the use of a Schottky diode on an external power supply in order to isolate a host's power source from the universal serial bus hub's power source as well as to signal the universal serial bus hub that an external power source is being applied.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

FIG. **1** labeled "Prior Art" represents a computer system with several peripherals attached thereto.

FIG. **2** is a perspective view of a universal serial bus having a host controller, a root hub and several peripherals in accordance with an embodiment of the present invention.

FIG. **3** is a schematic circuit diagram showing a seven port universal serial bus hub in accordance with an embodiment of the present invention.

FIG. **4** is a schematic view of a power supply that is suitable for use in the circuit shown in FIG. **3**.

FIG. **5** is a state flow diagram illustrating an example of the operation of the universal serial bus hub shown in FIG. **3**.

The use of the same reference symbols in different drawings indicates similar or identical items.

## DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

Universal Serial Bus (USB) is a new technology that changes the manner in which peripherals are connected to a

computer system. The specification for USB was developed by several computer hardware and software manufacturers in order to overcome the problems discussed above regarding the number of interfaces and connectors required for peripherals attached to personal computers. The USB Specification Revision 1.0, Compaq, Digital Equipment Corporation, IBM PC Company, Intel, Microsoft, NEC and Northern Telecom, Jan. 15, 1996, is expressly incorporated herein by reference ("USB Specification" or "Specification").

Under the USB Specification, compatible peripherals are selectively coupled to a computer system through a universal connector and socket for a universal serial bus. A universal four wire cable for transferring signal and power provides four signals including: Data+, Data−, 5 Volts, and Ground. The Specification provides that information is transmitted across the bus in "packets" with each packet having an address uniquely associated with a logical device, thereby allowing information packets from all linked devices to share the same bus.

USB supports sharing of a signal port among several devices in a hierarchical interconnection. An important part of the interconnection is the ability to plug in hubs with multiple connections, thereby allowing further branching of the hierarchical interconnection scheme. The USB Specification has no limit to the number of hubs and devices that can be connected to the bus, except that the number of addresses allowed by the protocol limits the number on one bus to 127. Given that hubs can be coupled to either another hub or to the host computer, host controller circuitry is present in both the host computer and the host hub. Hereinafter, therefore, the term "host controller" refers to either an upstream host hub controller or a host computer controller.

The hubs are responsible for power management, device support, and connection and disconnection detection among other supporting functions. The host controller provides at least one upstream port for connecting the hub to the host. The specification categorizes two kinds of hubs based on the source of power and the sinking requirements of the hub. The two kinds of hubs are bus-powered and self-powered. A bus-powered hub draws all power from the USB connector coupled to the host controller. Each port for a bus-powered hub supplies 100 mA of load to all downstream ports. A self-powered hub does not draw power from the USB connection, but draws power from another source, for example a power supply coupled to the hub. The Specification provides that self-powered hubs supply 500 mA of current to all external downstream ports. The Specification also identifies three different types of USB devices for use with the different types of hubs. These devices include low-power bus powered devices that draw no more than 100 mA at any time, high-power bus powered devices that draw no more than 100 mA on power up and up to 500 mA after configuration, and self-powered devices that draw up to 100 mA from their upstream connection for interface purposes when the hub is powered down.

FIG. **2** illustrates an embodiment of the present invention. FIG. **2** shows a computer system **20**, including a monitor **26**, a USB host controller **30** coupled to a USB port **32**, a USB hub **25**, and several peripherals coupled to the hub **25**. The host controller **30** allows both bus-powered and self-powered devices to operate on the same hub **25**. This is accomplished through circuitry shown in FIG. **3** and shown in FIG. **2** which connects between the host controller **30**, port **32**, coupled to the host controller **30**, the hub power supply **200** (FIG.4), and a USB Controller **110** located inside the hub **25**. The circuitry accomplishes the switching between the two modes of power operation between the host controller **30** and the hub **25** and peripherals coupled to the hub **25**. When a power supply coupled to the hub is powered on, the hub **25** will operate in self-powered mode. When the hub **25** is coupled to the host controller **30** and the hub power supply **200** is powered down, the hub **25** will switch to bus-powered mode. In contrast, when the hub **25** is in bus-powered mode and the power supply **200** is powered on, the hub **25** will switch to self-powered mode. The transition between these two modes is accomplished through logical switching circuitry and detection circuitry as represented in the schematic diagrams in FIG. **3** and FIG. **4**. The transition uses an operating method illustrated by the state diagrams shown in FIG. **5**.

FIG. **3** represents a schematic of the hub logic circuitry **600**, shown as the area bounded by the line from point A to point B which includes switching circuitry and detection circuitry, the USB Controller **110**, and other hub circuitry for USB connection to peripherals. The USB Controller **110** is known in the art and is represented in an exemplary system as part number TUSB2070, manufactured by TEXAS INSTRUMENTS™. FIG. **4** represents the power supply **200** coupled to the logic circuitry **600** through connector **100**. The power supply **200** is known in the art as a ST204A Power Supply manufactured by Power Integrations and is described in the Power Integrations, Inc. Data Book and Design Guide, 1996–97, incorporated herein by reference.

FIGS. **3** and **4** together demonstrate an embodiment in which the operating system and the host controller smoothly transition between running in bus-powered mode and self-powered mode. The circuit provides for this smooth transition through interrupting communication between the hub and the host controller through "global resets." The circuit sends a reset signal to the host controller **30** while at the same time providing a ramp-up time for the hub **25** to transition into either bus-powered mode or self-powered mode before allowing the hub **25** to once again receive data signaling. The logic circuitry **600** provides for the power source change while the data transmission from the host controller **30** through connector **111** is terminated and hub **25** is in a reset mode.

Operation of Automatic Switching

Referring to FIG. **3** and FIG. **4**, in combination, follow the 5 V_S signal on line **140** shown at connector **100**. The power supply **200**, shown in FIG. **4**, generates the signal on line **140** when the power supply **200** is powered on and enabled and pins **2** and **3** on connector **100** show 5 volts. The voltage on Pin **3**, signal line **140**, of connector **100** is "clamped" by the Zener diode **101** to produce 3.3 Volts. The presence of the signal line **140** causes three events to occur. First, a "global reset" occurs. Second, Pin **10** of the USB Controller **110**, "/Buspwr" **300** de-asserts thereby signaling that the USB Controller **110** is entering self-power mode. Third, power from the host controller **30** is removed thereby terminating bus-powered mode.

Removal of Bus-powered Mode

Bus-powered mode is terminated by disabling switch **116**, shown as part number TPS2041, which is a Power Switch used to switch the host controller **30** power bus onto the hub **25** power bus. Pin **4** of switch **116** controls the switch through an active low "Enable". The presence of a signal on line **140**, which is considered a logic "high", appears at Pin **4** of switch **116** when the power supply **200** is powered "on". Thus, switch **116** and a signal on line **140** function as both the switching circuitry and the detection circuitry. When signal **140** is not present, resistors shown in the logic

circuitry **600** electrically coupled to Pin **4** of switch **116**, such as resistor **310**, shown as 27 KOhms, provide a reference to ground. This provides a "Logic Low", thereby enabling switch **116**. Note that this system of switching power disables the power from the host controller **30** when self power is enabled, thereby preventing damage that could occur to the host computer **20**. Additionally, as discussed below, the system and method conveniently terminates bus-supplied power when the power supply **200** is powered on even when bus-powered mode is operational by reinitializing the hub **25** through "global reset."

Global Reset

Global reset refers to the global initialization or reinitialization of hub **25**. As explained below, global reset has several components, an approximately 0.4 second time dela, and two low voltage pulses, one with a pulse width of approximately 750 $\mu$ Secs used for resetting the hub after self-power is initiated, and one with a pulse width of approximately 2 $\mu$ Secs used for resetting the hub after self power is removed. These components reset the USB Controller **110** and communication of reset conditions with the host controller **30**.

Global reset occurs when a signal on line **140** is present and resistor **102** begins to charge capacitor **103**, whose voltage is seen at comparator **104**'s noninverting input, Pin **3**. This is called the Primary Time delay and is approximately 0.4 seconds. This 0.4 second time delay allows the +5 Volts on Pin **2** of Connector **100** from the Power Supply **200** to stabilize. When the voltage across capacitor **103**, which is coupled to the noninverting input of comparator **104**, Pin **3**, passes the voltage level at the inverting input of comparator **104**, Pin **2**, the comparator **104** switches its output located at Pin **1** from a "Low" to a "High" voltage. The voltage divider made up of resistor **105** and resistor **106** assures that the voltage at the inverting input of comparator **104**, Pin **2** is higher then the voltage at the noninverting input of comparator **104**, Pin **3** prior to the presence of signal **140**. Therefore, comparator **104** output Pin **1** will be "Low" (an initial condition) prior to the signal **140** presence.

The resistor-capacitor network pairs including resistor **108** and capacitor **109**, and resistor **120** and capacitor **121**, are positive feedback elements preventing oscillations from the slow rising voltage across capacitor **103**.

The output voltage of comparator **104**, Pin **1** reaches capacitor **180** and resistor **112**. At the time just after switching, the output voltage of comparator **104**, Pin **1** reaches resistor **112**. Resistor **112** is coupled with the Pin **6** of comparator **107**, the inverting input. When this voltage (3.3 V) appears at comparator **107**, Pin **6**, Pin **7** of comparator **107** switches from a "High" to a "Low." The voltage divider made up of resistors **105** and **106** assures that the voltage at Pin **5** of comparator **107** is higher then the voltage at Pin **6** of comparator **107** prior to the presence of signal **140**. Thus, Pin **7** of comparator **107** exhibits a "High" thereby indicating an initial condition and no reset to USB Controller **110** before signal **140** appears. As time goes on, capacitor **180** charges and the voltage across resistor **112** reduces. After approximately 750 $\mu$ Secs, the voltage at resistor **112**, which is coupled to the inverting input of comparator **107**, is less than the voltage appearing at the noninverting input, Pin **5** of comparator **107**, thereby switching the output of comparator **107**, Pin **7** back to 3.3 Volts. Note that this is a low voltage pulse with a pulse width of approximately 750 $\mu$ Secs. discussed above, and that the pulse begins approximately 0.4 seconds after the power supply **200** is powered "on" and "Self Power" is enabled. This pulse resets the USB Controller **110**.

Another component of global reset concerns communication of the hub **25** with the host Controller **30**. The logic circuitry **600** signals to the upstream host Controller **30** that a device is attempting to enumerate. Enumeration refers to attaching and requesting initialization from the host Controller **30**. The logic circuitry **600** accomplishes this using a resistor **320** coupled to the reset line of the USB Controller **110**, Pin **25**. Resistor **320** electrically couples to the gate of MOSFET Transistor **113**. Note that a bipolar junction transistor may replace the MOSFET, in which case resistor **320** couples to the base of the bipolar transistor. Further, if a bipolar junction transistor is used, the connection between resistor **320** and voltage source **130** would not be an open circuit, but would be closed with an additional resistor added. When there is voltage of 3.3 volts on resistor **320**, the MOSFET Transistor **113** drives transistor **113** to the "on" state, which then provides a path for a 3.3 volt signal through pull-up resistor **123** onto the upstream port of connector **111**, Pin **3**, shown as "Data+."

The presence of a voltage at pull up resistor **123** signals to the upstream host **30** that a device is trying to enumerate. When transistor **113** disables, the host **30** considers the device to be disengaged, thereby releasing the upstream of connector **111** port for a new device to attach. Thus, when the reset line, Pin **25** of the USB controller **110**, is enabled (logic "low"), the host Controller **30** releases the port to which the hub **25** is attached. When the reset line is disabled (logic "high") the host Controller **30** re-enumerates, thereby attaching the hub **25**. This attaching and detaching is how the hub **25** identifies itself as a self or bus-powered device to the operating system of computer **20**.

Before the global reset discussed above occurs, the 3.3 volts developed across the Zener diode **101** is also at Pin **4** of Switch **116** as well as at Pin **10** of the USB Controller **110**. The input pins of switch **116** connect to the 5 Volts, the power supplied from the host controller through connector **111**. When Pin **4** of switch **116** reaches 3.3 volts, the switch **116** opens and the input signals of switch **116**, at Pins **2** and **3**, are removed from Pins **7** and **6**, respectively. This acts to prevent the host controller **30** from powering the hub. Pin **10** of the USB Controller **110** functions to signal the USB Controller that the hub is in self-powered mode. The USB Controller does not recognize that the hub is in self-powered mode until 0.40075 seconds later.

Global Reset When Exiting Self-Power Mode

When the hub **25** operates in self-powered mode and self power terminates, the hub **25** reverts to the host Controller **30** supplied power and performs a global reset. The global reset occurs when exiting self-powered mode and entering bus-powered mode. Terminating self power means terminating the signal on line **140**, discussed above. When power is not provided through the power supply **200**, the power discharges from the resistor-capacitor network of resistor **102** and capacitor **103** through resistor **310** and other resistors in parallel with resistor **310** to ground. When the voltage at capacitor **103**, which couples to the non inverting input, Pin **3** of comparator **104**, passes the voltage at the inverting input, Pin **2** of comparator **104**, the output, Pin **1** of comparator **104** goes to zero volts, or ground. When Pin **1** goes to ground, the resistor-capacitor network of capacitor **180** and resistor **112** discharges through the path created. Because capacitor **180** is fully charged when Pin **1** of comparator **104** goes to ground, a negative voltage is produced across resistor **112** and across the inverting input of comparator **107**, Pin **6**. A negative voltage at comparator **107** input overrides the normal operation of comparator **107** and sends the signal at output Pin **7** to ground, as long as the

comparator **107** input is a large negative voltage. This feature of comparators makes for an efficient circuit that avoids additional circuitry. It is because of this feature of comparators that a reset is generated when self power is terminated. The length of the reset pulse is approximately 2 $\mu$ Secs. This 2 $\mu$ Secs. is the length of time the negative voltage at Pin **5** of comparator **107**, the noninverting input, is close to its maximum.

Global Reset During Bus-Powered Mode

Global Reset occurs during bus-powered mode through switch **116**. Switch **116** asserts reset of the USB Controller **110**, Pin **25** when its input voltage, shown as the 5 V-S Pin **1** of connector **111**, stabilizes. The output lines, shown as Pins **6**, **7** and **8**, of Switch **116** regulate the 3.3 volts that powers the USB Controller **110** and its associated circuitry. Note that the 3.3 volts output from switch **116** is not the 3.3 volts from the 5 Volts line, Pin **1** of connector **111**. Switch **116** first stabilizes the 3.3 volts and then releases the Reset line on the USB Controller **110**.

Operation of Power Supply

Referring to FIGS. **3** and **4** together, note that when the power from the power supply **200** is removed, it appears that power is being supplied to the power supply through pin **2** of connector **100** from switch **116**, pin **8**. This is not the case. In order to prevent power from being routed to the power supply **200**, the power supply **200** circuit is equipped with a Schottky-barrier diode **250**, shown as part number MBR1635, which acts to prevent any voltage from passed beyond the Schottky-barrier diode **250** on the power supply **200** from the hub **25**. The power supply is a conventional flyback switching power supply with an adjustable output voltage and voltage and power rectifiers. The power supply **200** is a so-called "offline switcher" that switches the higher 110 Volt line from its power source, and does not switch a low voltage from a transformer, as might be seen in other power supplies. Other power supplies not referenced here can be substituted by those skilled in the art and still be within the scope of an embodiment presented herein.

Example

Switching from Bus-Powered Mode to Self-Powered Mode

With reference to FIG. **3**, in combination with FIG. **2**, an example of how the logic circuitry **600** communicates with the host controller **30** and USB Controller **110** indicating that the hub **25** switched from a bus-powered mode to a self-powered mode is presented. In this example, hub **25** is first initialized to bus-powered mode. Peripheral devices, in this example represented by a scanner **21** and a modem **22**, are attached to hub **25**. The power supply **200** coupled to the hub **25** is powered on. According to an embodiment described above, supplying power to the power supply **200** places the USB Controller **110** into reset mode, thereby automatically relaying to the operating system of the host controller **30** an indication to terminate data transmittal. This occurs even if the hub **25** was running in bus-powered mode at the time the power supply **200** is powered on.

Referring to FIGS. **3** and **4**, when the power supply **200** is powered on, the voltage at connector **100** is routed through Zener diode **101** to switch **116** and at the same time routed indirectly to capacitor **180** through comparator **104**. The voltage from the Zener diode **101** immediately reaches Switch **116** and the USB Controller **110** pin **10**, "/Buspwr", shown as a "Not" enabled switch. Thus, the USB Controller will no longer be in bus-powered mode when the Zener diode **101** is activated upon powering up of the power supply **200** and the USB Controller **110** receives a reset signal.

Example

Switching from Self-Powered Mode to Bus-Powered Mode

With reference to FIGS. **3** and **4**, an example of how the logic circuitry **600** communicates with the host controller **30** and the USB Controller **110** to indicate that hub **25** switched from a self-powered mode to a bus-powered mode is presented. In this example, hub **25** is first initialized to self-powered mode with the power supply **200** powered on. After hub **25** is initialized to self-powered mode, the power supply **200** is powered down, but the hub **25** remains coupled to the host controller **30** through connector **111**. According to an embodiment described above, removing power from the power supply **200** puts the USB Controller **110** into reset mode, thereby automatically relaying to the operating system of the host controller **30** to suspend data transmittal.

When the power supply **200** is powered down, switch **116** is enabled and capacitor **180** will no longer be charged via comparator **104**. As stated above with reference to the example of switching from bus-powered mode to self-powered mode, the voltage from the Zener diode **101** will immediately reach the USB Controller **110** pin **10**, "/Buspwr" and will switch the USB Controller **110** into bus-powered mode when the reset is asserted.

Time Delay Added to Delay Over Current Pin from Triggering

Referring to FIG. **3**, the following resistor-capacitor pairs: **380** and **356**; **381** and **357**; **382** and **358**; **383** and **359**; **384** and **340**; **385** and **341**; **386** and **342** provide a time delay before triggering an over-current condition to the USB Controller **110**. The time delay prevents devices attached to the hub **25** that have large input capacitors from appearing temporarily as shorts to switches **116** and **350**. As these large input capacitors charge, the switches **116** and **350** output an overcurrent warning signal (/overcurrent=0 volts). This overcurrent condition begins to discharge its associated capacitors listed above. After the large input capacitors charge up, the resistor-capacitor pairs begin to charge back to their "high" logic level state and the USB Controller **110** never sees the warning signal. If a true short exists, then the resistor-capacitor pairs will discharge completely and the USB Controller **110** will disable the respective switch. Other components shown in FIG. **3** and not described herein are conventional USB hub circuitry, including, for example, components for purposes of connecting peripherals attached to the hub **25** through the USB Controller **110**.

Method of Operation

Referring to FIG. **5** in combination with FIGS. **3** and **4**, a state flow diagram is represented showing the manner in which a hub **25** built according to an embodiment of this invention would transition between bus-powered mode and self-powered mode. The first step **300** in the state machine (e.g. a computer program resident in and executed by USB Controller **110** in conjunction with logic circuitry **600**) relates to determining whether or not power supply **200** is supplying power to the hub **25**. If power supply **200** supplies power to hub **25**, indicating step **302**, then, as shown in step **306**, the USB Controller **110** will initialize hub **25** as a self-powered hub by putting the hub **25** into reset cycle. Steps **310**, **314**, **318**, **322** and step **326** provide the steps taken by the logic circuitry **600** for initializing the hub **25** for self-powered mode. Steps **310** and **314** provide for a first resistor-capacitor timer, shown in FIG. **3** by the resistor-capacitor pair **102** and **103**, to begin a timing sequence by charging to a specified value in accordance with the timing cycle and then discharging. Steps **318** and **322** provide for the second resistor-capacitor timer, shown in FIG. **3** as the resistor-capacitor pair **112** and **180** to begin timing sequence

by charging to the A. specified value in accordance with the timing cycle and then discharging. The next step, step **326**, provides that the hub **25** is taken out of reset. At this point, if the hub **25** was not previously coupled to a host controller **30**, and then hub **25** was later coupled to a host controller **30**, the self-powered mode would take precedence over bus-powered mode. Thus, as indicated in step **332**, the power from an upstream bus is ignored.

If the power supply **200** is not powered on, the hub **25** will check for power according to step **300** from an upstream host, as shown in step **304**. Once power is received from an upstream host, step **308** provides that the hub **25** will go into reset mode. Next, in step **312**, switch **115**, as shown in FIG. **3**, will perform the reset cycle by holding the hub **25** in reset until power stabilizes. In step **316**, the hub **25** will be "on" with reset de-asserted. At this point, if the power supply **200** is powered on, as in step **320**, the hub **25** initializes, as indicated in step **324** to self-powered mode. As shown, self-powered mode will take precedence over bus-powered mode. Once the hub **25** is initialized, the hub is ready for peripherals to be attached as in steps **328** and **334**.

While the invention has been described with reference to various embodiments, it will be understood that these embodiments are illustrative and that the scope of the invention is not limited to them. Many variations, modifications, additions and improvements of the embodiments described are possible. For example, one skilled in the art could apply the information contained herein to serial bus hubs in general as well as to universal serial bus hubs.

Variations and modifications of the embodiments disclosed herein may be made based on the description set forth herein, without departing from the scope and spirit of the invention as set forth in the following claims.

What is claimed is:

**1**. A bus hub for connection via a serial bus to a serial bus host hub, the bus hub comprising:

a serial bus hub having a connector to a power supply, the serial bus hub also receiving power from the serial bus host hub;

a bus controller coupled to the serial bus hub; and

a switch coupled to the bus controller and to the power supply, wherein the switch switches the bus hub between being powered by the power supply and being powered by the power from the serial bus host hub.

**2**. The serial bus hub of claim **1** wherein the serial bus is a universal serial bus; the serial bus hub is a universal serial bus hub; and the serial bus host hub is a universal serial bus host hub.

**3**. The serial bus hub of claim **1**, wherein the serial bus host hub is one of a serial bus host hub in a computer and a serial bus host hub in a computer peripheral.

**4**. The serial bus hub of claim **1**, wherein:

the power supply connected to the serial bus hub provides power to the serial bus hub in a self-powered mode, and the serial bus host hub provides power to the serial bus hub in a bus-powered mode;

the switch switches the mode of operation between the self-powered mode and the bus-powered mode when one of a signal from the power supply to the serial bus hub indicates that the power supply is available to the serial bus hub and a signal from the power supply to the serial bus hub indicates that power from the power supply is unavailable to the serial bus hub; and

the signal that power is unavailable from the power supply to the serial bus hub is the indication to change modes when the serial bus hub is running in the self-powered mode.

**5**. The serial bus hub of claim **1**, wherein:

the serial bus controller coupled to the serial bus hub initializes the serial bus hub upon receiving the signal that power is unavailable from the power supply and upon receiving the signal that power is available from the power supply.

**6**. The serial bus hub of claim **1**, further comprising:

at least one timer circuit coupled via a connector to the power supply, wherein the timer circuit provides a delay for power supplied to the serial bus hub to stabilize prior to the initializing of the serial bus hub, and the timer circuit outputs a low voltage pulse to reset the bus controller.

**7**. The serial bus hub of claim **6** wherein the low voltage pulse has a pulse width of approximately 750 $\mu$ Secs. and begins approximately 0.4 seconds after the power supply begins supplying power to the serial bus hub.

**8**. The serial bus hub of claim **6** wherein the at least one timer circuit is a resistor-capacitor timer.

**9**. The serial bus hub of claim **1** further comprising:

a plurality of connectors coupled to the serial bus hub, the plurality of connectors being adapted for detachably coupling a plurality of peripherals to the serial bus hub.

**10**. The serial bus hub of claim **1** wherein the switch comprises a field effect transistor.

**11**. The serial bus hub of claim **1** wherein the switch comprises a bipolar junction transistor.

**12**. The serial bus hub of claim **1** wherein the switch comprises a plurality of switches electrically coupled to a serial bus.

**13**. The serial bus hub of claim **1**, further comprising:

logic circuitry that communicates reset commands to the bus controller, the logic circuitry including at least one comparator, at least one Zener diode, at least one voltage dividing circuit, and at least one timer circuit, the Zener diode electrically coupled to the power supply and the at least one comparator, the at least one comparator also being electrically coupled to the at least one timer circuit and the at least one voltage dividing circuit.

**14**. The serial bus hub of claim **13**, wherein the power supply is coupled to the logic circuitry via a connector, the power supply comprising:

a flyback switching power supply; and

a Schottky-barrier diode, the Schottky-barrier diode being in the flyback switching power supply to prevent power from the serial bus hub from entering the power supply past the Schottky-barrier diode.

**15**. A system for controlling communication and power in a serial bus comprising:

a serial bus hub adapted to detachably couple at least one peripheral to a computer system, the computer system including a processor, a memory, and a serial bus host hub capable of delivering power to the serial bus hub;

a power supply electrically coupled to the serial bus hub, the power supply capable of delivering power to the serial bus hub;

a bus controller coupled to the hub, wherein the bus controller receives signals from the computer system through the serial bus, and the bus controller receiving signals from the serial bus hub; and

a switch coupled to the bus controller and to the power supply, wherein the switch switches the serial bus hub between being powered by the power supply and being powered by the power from a serial bus host hub.

16. The system of claim 15 wherein the switch comprises a field effect transistor.

17. The system of claim 15 wherein the switch comprises a bipolar junction transistor.

18. The system of claim 15 wherein the serial bus is a universal serial bus; the serial bus hub is a universal serial bus hub; and the serial bus host hub is a universal serial bus host hub.

19. The system of claim 15, wherein the serial bus host hub is one of a serial bus host hub in a computer; and a serial bus host hub in a computer peripheral.

20. The system of claim 15, further comprising:

logic circuitry coupled to the switch, wherein the logic circuitry initializes the serial bus hub to a first mode, the first mode being one of self-powered mode in which the serial bus hub is powered by the power supply and bus-powered mode in which the serial bus hub is powered by the power supplied by the serial bus host hub, wherein the logic circuitry detects whether the power supply is powered on, and the logic circuitry then initializes the serial bus hub to self-powered mode if the first mode is bus-powered mode.

21. The system of claim 20, wherein the logic circuitry includes:

at least one timer circuit coupled to the power supply via a connector, the at least one timer circuit being responsive to signaling from the power supply, the at least one timer circuit providing a delay for power supplied to the serial bus hub to stabilize prior to the logic circuitry initializing the serial bus hub, and wherein the at least one timer circuit outputs a low voltage pulse to reset the bus controller.

22. The system of claim 20, wherein the logic circuitry includes:

a Zener diode coupled to the switch, the Zener diode further electrically coupled to the power supply, the Zener diode clamping the signal voltage from the power supply; and

a plurality of voltage dividing circuits coupled to the Zener diode and the at least one timer circuit, the at least one timer circuit including a plurality of comparators electrically coupled to the plurality of voltage dividing circuits, the plurality of comparators outputting a reset signal to the bus controller when a change in power mode occurs.

23. The system of claim 15 wherein the power supply comprises:

a flyback switching power supply; and

a Schottky-barrier diode, the Schottky-barrier diode being in the flyback switching power supply to prevent power from the serial bus hub from entering the power supply past the Schottky-barrier diode.

24. The system of claim 15 wherein the power supply further comprises an offline switcher.

25. A method for communicating and for control of power in a serial bus hub that detachably couples a plurality of peripherals to a computer, the computer including a host hub powered by the computer, the serial bus hub being coupled to a power supply, the method comprising:

determining whether the serial bus hub is receiving power from the power supply;

if the serial bus hub is receiving power from the power supply, initializing the serial bus hub to receive power from the power supply;

if the serial bus hub is not receiving power from the power supply, initializing the serial bus hub to receive power from an upstream serial bus host hub coupled to the serial bus hub; and

supplying power to the plurality of peripherals coupled to the hub.

26. The method of claim 25 wherein the serial bus hub is a universal serial bus hub; and the upstream serial bus host hub is an upstream universal serial bus host hub.

27. The method of claim 25 wherein the upstream serial bus host hub is one of a serial bus host hub in a computer and a serial bus host hub in a computer peripheral.

28. The method of claim 25 further comprising:

after initializing the serial bus hub to receive power from an upstream serial bus host hub, detecting that the power supply has been powered on; and

initializing the serial bus hub to receive power from the power supply coupled to the serial bus hub.

29. The method of claim 25 further comprising the steps of:

detecting that the power supply has been powered off; and

with the serial bus hub in a self-powered mode, reinitializing the serial bus hub to receive power from the upstream serial bus host hub upon detecting the power supply has been powered off.

30. The method of claim 25 further comprising:

detecting that the power source from the serial bus host hub has been powered off; and

with the serial bus hub in a bus-powered mode, powering down the serial bus hub.

31. The method of claim 25 further comprising:

detecting that the power source from the serial bus host hub has been powered off;

switching the serial bus hub to self-powered mode; and

providing power to the serial bus hub from the power supply.

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